LC77700B

(PowerPC 405IAP Embedded Processor)

User's Manual

OPBR

(Opb to Plb BRidge)

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Contents

About This Book

This book begins with an overview followed by detailed information on OPB to PLB bridge core signals, interfaces, registers, timing and operations.

The OPB to PLB bridge core features:

- Serves as OPB slave device and/or PLB master device
- Can be mapped to any OPB address space.
- As a 64-bit PLB master interface it supports
  - doubleword (64-bit) reads, and
  - doubleword, word, halfword, and byte writes
- Provides data packing on writes, up to 4-doublewords
- Accomodates fixed length burst (4 doubleword) prefetching for reads.
- Operates at 50+ MHz OPB clock frequency
- Supports PLB at 1, 2, 3, or 4 times the frequency of the OPB
- Utilizes clock and power management

Who Should Use This Book

This book is for hardware, software, and application developers who need to understand and system-on-a-chip (SOC) designs. The audience should understand embedded system design, operating systems, and the principles of computer organization.

Chapter 1. OPB to PLB bridge Overview

The OPB to PLB bridge is a soft core which enables transfers of data between the on-chip peripheral bus (OPB) and the processor local bus (PLB) under the direction of OPB master devices. The OPB to PLB bridge is a slave on the OPB and a master on the PLB. The OPB-toPLB bridge core is required for any application using the OPB master devices that access system resources on the PLB.

An application that comprises an OPB and a PLB can operate in the OPB mode. In OPB mode, the OPB to PLB bridge uses the OPB_fwXfer, OPB_hwXfer, and OPB_ABus(30:31) to decode requested data sizes. In OPB mode, the code will only respond properly to byte, aligned halfword, and fullword transfers, as defined by the OPB architecture.

Features of the OPB to PLB bridge Include:

- Serves as OPB slave device and/or PLB master device
- Can be mapped to any OPB address space.
- As a 64-bit PLB master interface it supports
  - – doubleword (64-bit) reads, and
  - – doubleword, word, halfword, and byte writes
- Provides data packing on writes, up to 4-doublewords
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- Operates at 50+ MHz OPB clock frequency
- Supports PLB at 1, 2, 3, or 4 times the frequency of the OPB
- Utilizes clock and power management

Figure 1 demonstrates how the OPB to PLB bridge is inter connected for the purpose of system-on-a-chip design.

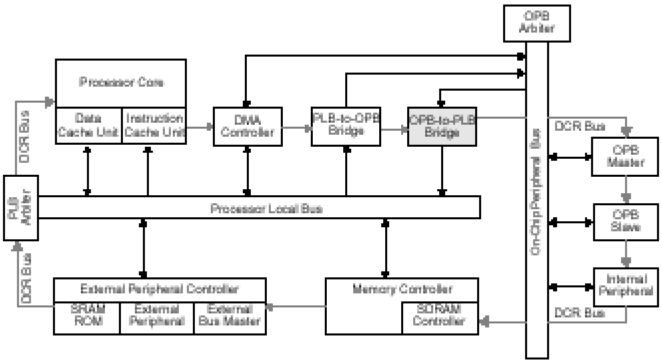

Figure 1. OPB to PLB bridge Interconnection

As shown in Figure 1, the on-chip bus structure provides a link between the processor core and other peripherals which consist of PLB and OPB master and slave devices.

The processor local bus (PLB) is the high performance bus used to access memory through the bus interface units. The two bus interface units shown above: external peripheral controller and memory controller are the PLB slaves. The processor core has two PLB master connections, one for instruction cache and one for data cache. Attached to the PLB is also the direct memory access (DMA) controller, which is a PLB master device used in data intensive applications to improve data transfer performance.

Lower performance peripherals (such as OPB master, slave, and other internal peripherals) are attached to the on-chip peripheral bus (OPB). A bridge is provided between the PLB and OPB to enable data transfer by PLB masters to and from OPB slaves. In the above example we have two bridges, a PLB-to-OPB bridge which is a slave on the PLB and a master on the OPB and an OPB to PLB bridge which is a slave on the OPB and a master on the PLB. OPB peripherals may also comprise DMA peripherals.

The device control register (DCR) bus is used primarily for accessing status and control registers within the various PLB and OPB masters and slaves. It is meant to off-load the PLB from the lower performance status and control read and write transfers. The DCR bus architecture allows data transfers among OPB peripherals to occur independently from, and concurrent with, data transfers between the processor and memory, or among other PLB devices.

Figure 2 provides a block diagram of the OPB to PLB bridge.

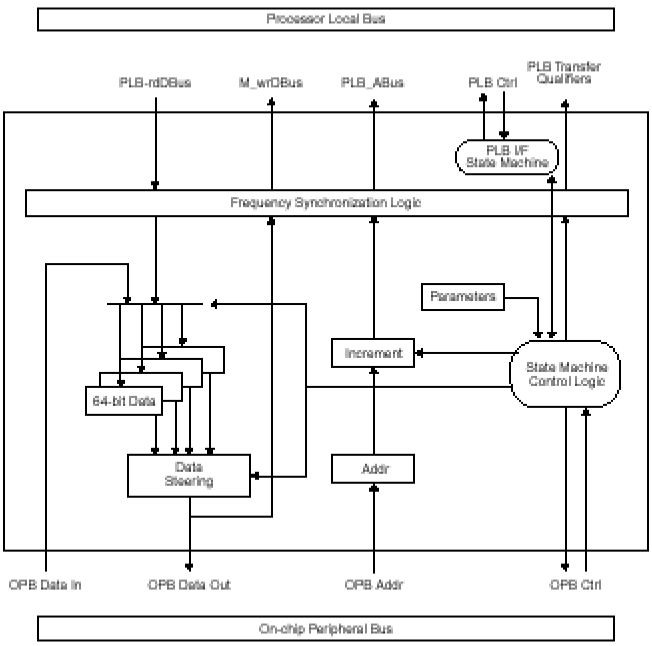

Figure 2. OPB to PLB bridge Block Diagram

1.1 PLB Interface

The OPB to PLB bridge interfaces to the PLB as a 64-bit master device cas PLB architecture. It supports all single write transfers, and fixed-length doubleword write bursts. It performs a doubleword read to service all single read requests, and fixed length doubleword read burst to service read burst requests. The OPB to PLB bridge synchronizes data transfers between the PLB and OPB clock domains. This synchronization techique supports PLB to OPB frequency ratios of 4:1, 3:1, 2:1 and 1:1.

1.2 OPB Interface

The OPB to PLB bridge interfaces to the OPB as a 32-bit slave device. It is selected by an externally decoded select line, so that the PLB slaves may be mapped anywhere in the OPB address map.

1.3 Address Registers

The OPB to PLB bridge contains a single 32-bit OPB address and transfer qualifier register. Addresses are incremented as necessary to affect transfers on the PLB.

1.4 Clock and Power Management

Power consumption within the OPB to PLB bridge is reduced by gating the clock to all latches internally. Minimum power is achieved when no active PLB requests are pending, the data buffer is empty, and the OPB is idle.

In addition, a sleep request signal is available to a central clock and power management unit (CPM) module. This signal is asserted by the OPB to PLB bridge to indicate when it is permissible to shut off its clocks.

1.5 Internal Data Buffer Structure and Operation

The OPB to PLB bridge contains a 32-byte data buffer, used for both read and write operations. During write operations, the buffer is organized as a 4-doubleword FIFO. During read operations, the buffer is organized as a fully associative cache with a line size of one fullword.
Operation of the buffer differs for both read and write requests depending on the state of the OPB_seqAddr signal.

1.5.1 OPB_seqAddr Deasserted

All non-seqAddr read operations on the OPB generate a single doubleword read on the PLB. The requested read data is provided from within the doubleword, and subsequent read addresses are checked to see if they may be serviced from the buffer.
Non-seqAddr write operations on the OPB are acknowledged and performed directly on the PLB at the size indicated (i.e., byte, halfword, or fullword). In external bus master mode, three-byte and unaligned halfword transfers are also supported.

1.5.2 OPB_seqAddr Asserted

All seqAddr read requests result in a PLB 4 doubleword fixed length burst, beginning at the doubleword in which the requested data is found. The requested read data is provided from within the doubleword, and subsequent read addresses are checked to see if they may be serviced from the buffer.
All seqAddr write requests result in packing of the data in the buffer and emptying it when full using fixed-length bursts, until a write for which seqAddr is not asserted, when all remaining data in the buffer are written on the PLB in the most efficient manner possible. Nonaligned data are first packed up and written to achieve doubleword alignment. Write data are then packed into the buffer until full, and the buffer written using 4-doubleword fixed-length burst protocol. This process repeats until a write request is received with seqAddr deasserted, at which point the buffer is flushed of remaining write data, using the most efficient cycles available.
The OPB to PLB bridge handles PLB slave burst termination and 32-bit conversion cycles as per PLB architecture.

Chapter 2. OPB to PLB bridge Registers

From a programming perspective, there are two accessable registers residing in the OPB to PLB bridge. These are the Bridge Control Register (GCTRL) and the Bridge Status Register (GSTAT). Table 6 provides a summary of all OPB to PLB bridge registers which are discussed in detail in this section.

Table 6. OPB to PLB bridge Registers

Mnemonic	Register Name	Decode	Access
GCTRL	Bridge Control Register		Read/Write
GSTAT	Bridge Status Register		Read-Only

2.1 Bridge Control Register (GCTRL)

The Bridge Control Register (GCTRL) contains the control bits for the OPB to PLB bridge core. It is read from and written to via the DCR bus. Figure 9 shows GCTRL bit definitions.

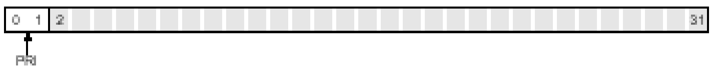

Figure 9. Bridge Control Register (GCTRL)

0:1	PRI	PLB Priority Bits Determines the priority of PLB requests. Reset to value "2'b11" These bits determine the priority of PLB requests. They are directly connected to the PLB_priority(0:1) bits during a PLB request. During reset, these bits are set to the value "2'b11"
2:31		Reserved

2.2 Bridge Status Register (GSTAT)

The Bridge Status Register (GSTAT) contains the error bit for the OPB to PLB bridge core. To clear the status register, a "1" must be loaded into those register bits that are to be cleared. Writing a "0" to any bit in the status register will not affect the state of the bit.
Figure 10 shows the GSTAT bit definitions.

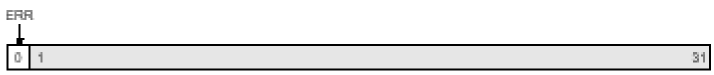

Figure 10. Bridge Status Register (GSTAT)

0	ERR	Error Bit Reset to 0
1:31		Reserved

2.2.1 Error Bit

The error bit is set whenever a PLB slave reports an error to the OPB to PLB bridge. For read transfers, the error is additionally reported to the OPB master through BGI_errAck. For posted single writes and errors occuring after the deassertion of OPB_seqAddr on burst writes, no error is reported to the OPB master. An error is reported to the OPB master through BGI_errAck for a previous write error if OPB_seqAddr is still asserted (but note that the error does not correspond to the transfer being currently processed).
The OPB to PLB bridge status register error bit should be polled to detect errors, and the PLB-to-OPB Bridge Error Address Register (GEAR) and PLB-to-OPB Bridge Error Status Register (GESR) of the PLB slave consulted for details of the error condition. The GEAR records the address where the error occurred and the GESR records the error type and the master involved in

the error.

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