

LC77700B

(PowerPC 405IAP Embedded Processor)

User's Manual

OPB ARB

(OPB ARBiter)

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About this Book

This book provides an overview and register descriptions for the On-Chip Peripheral Bus (OPB) Arbiter.

Who Should Use This Book

This book is for hardware, software, and application developers who need to understand the OPB Arbiter.

Chapter 1. On-Chip Peripheral Bus Arbiter (4 Master)

1.1. Introduction

The on-chip peripheral bus (OPB) arbiter is an internal 32-bit address and 32-bit data bus core designed for on-chip peripheral integration. This document is organized as follows:

- OPB Arbiter Overview
- OPB Arbiter Register Descriptions

1.2. OPB Arbiter Overview

The OPB arbiter has the following features:

- OPB slave interface
- OPB arbitration consisting of:
 - Control and priority registers
 - Priority register update logic
 - Arbitration logic
- Park/Grant logic (including GrantLast register)
- Watchdog timer
- Arbitrates for OPB resources among up to four bus masters
- Arbitration priorities among master devices programmable via register write
- Optional dynamic priority reordering mode, implementing a true least recently used (LRU) algorithm.
- Two optional bus parking modes for reduced access latency when no master devices are requesting:
 - Park on selected OPB master device (via register write)
 - Park on last OPB master which was granted OPB access
- Compliant with the on-chip peripheral bus specification.

Figure 1 provides a functional block diagram of the OPB arbiter.

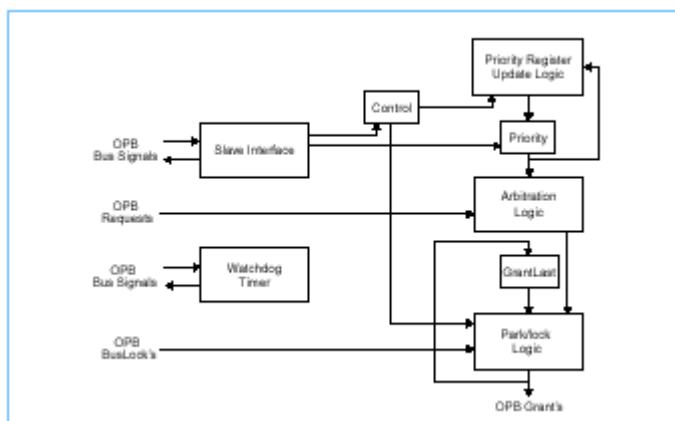


Figure 1. OPB Arbiter Functional Block Diagram

1.3. OPB Slave Interface

The OPB arbiter is a byte-wide slave device on the on-chip peripheral bus. Its address in the OPB memory map is determined by the upper twenty six most significant bits (MSb) of the OPB address bus. The MSb of the OPB address bus are compared to this value during valid OPB transfer cycles. If there is a match, the lower six least significant bits (LSb) are used to index one of the core's addressable registers for read and write operations.

1.4. OPB Arbitration

The arbitration section is the heart of the OPB arbiter. Arbitration is performed among up to four incoming request signals. One of the four possible active requests is preliminarily granted control of the OPB, based on the values of fields in the Priority Register (PR).

The Priority Register (PR) may be set by software, and it may optionally be autonomously updated following every arbitration cycle. Update of the Priority Register (PR) is controlled by fields in the Condition Register (CR).

1.5. Park/Lock Logic

Following the arbitration logic, the preliminary Grant signals are processed to implement the OPB bus parking and bus locking features. The actual Grant's out to the OPB master devices are registered to track current ownership of the OPB.

If the currently granted OPB master locks the bus, other masters' Grant signals are gated off, locking out arbitration of the bus.

If no master is currently Granted, the OPB Arbiter may assert the Grant for a particular master (either the last one Granted or a specific master identified in the Condition Register (CR)). This is referred to as parking the bus on that master. Parking reduces system latency by avoiding the need for the parked master to perform an arbitration cycle prior to proceeding with an OPB transaction. If a competing, higher priority master device issues a Request, the parked Grant signal is deasserted and the other master's Grant is asserted.

1.6. Watchdog Timer

The OPB arbiter contains the watchdog timer for the OPB to monitor the OPB control signals. If any OPB master device initiates an OPB transfer and does not receive a valid acknowledgment within 16 cycles, and the addressed slave device does not assert its time-out suppress signal within the 16 cycles, the watchdog timer will assert the OPB_timeout signal for one cycle. Each OPB master is responsible for responding to the timeout error signal appropriately. See On-Chip Peripheral Bus specification for details on timeout and time-out Suppression.

1.7. Reset Considerations

A logic "1" placed on the reset input while the clock is running causes all OPB arbiter registers to load their reset values. To complete the reset sequence, the reset input must be held at a logic "1" for a minimum of two OPB arbiter clock cycles.

Chapter 2. OPB Arbiter Register Descriptions

The OPB arbiter contains two registers accessible through its OPB slave Interface: the Priority Register and the Control Register.

The registers are accessed through normal OPB R/W operations. The registers within the arbiter are assigned addresses within its 64 byte space.

Table 5 provides a summary of all OPB arbiter registers which are discussed in detail in this section.

Table 5: OPB Arbiter Registers

Register Name	Decode(26:31)	Access
Priority Register	0x0	Read/Write
Control Register	0x1	Read/Write

2.1. Priority Register

The four “slots” of the Priority Register hold the master IDs of the attached master devices. Each master’s relative priority is determined by its ID’s location within this register. For example, for the Priority Register default (reset) value: 00 01 10 11, master 0 has the highest priority, and master 3 has the lowest priority.

The values of the priority fields of the Priority Register must be unique, that is, the same master ID cannot be loaded into more than one field of the Priority Register.

The Priority Register can be read via the arbiter’s slave interface, and is loaded via the slave interface or through the operation of dynamic priority mode.

Figure 14 shows the Priority Register bit definitions.

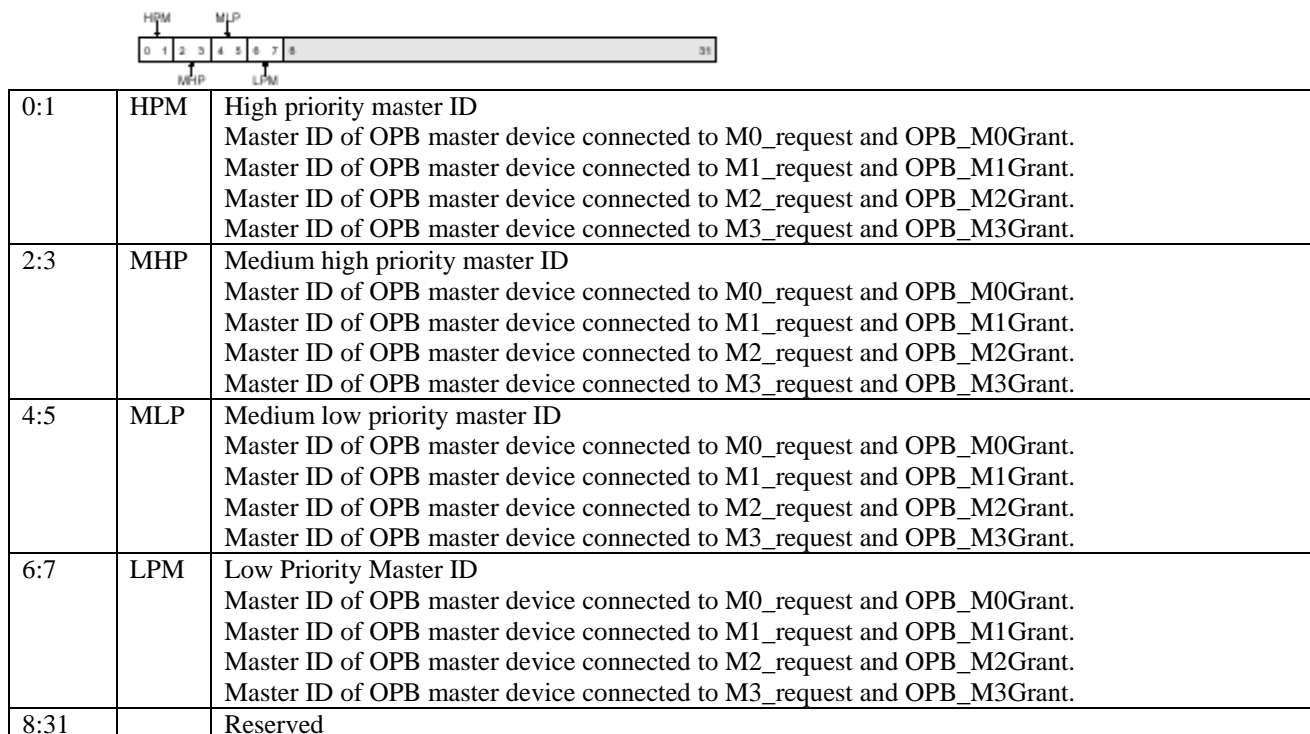
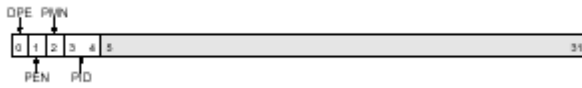


Figure 14. Priority Register

2.2. Control Register

Update of the Priority Register discussed above is controlled by fields in the Control register. Figure 15 shows the Control Register bit definitions.



0	DPE	Dynamic priority enable Dynamic priority disabled Dynamic priority enabled
1	PEN	Park enable Park disabled Park enabled
2	PMN	Park on master not last Park on master last Park on master not last
3:4	PID	Parked master ID Master ID of OPB master device connected to M0_request and OPB_M0Grant. Master ID of OPB master device connected to M1_request and OPB_M1Grant. Master ID of OPB master device connected to M2_request and OPB_M2Grant. Master ID of OPB master device connected to M3_request and OPB_M3Grant.
5:31		Reserved

Figure 15. Control Register



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