

LC77700B

(PowerPC 405IAP Embedded Processor)

User's Manual

POBR

(Plb to Opb BRidge)

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About This Book

This book begins with an overview followed by detailed information on PLB to OPB bridge core signals, interfaces, registers, timing and operations.

The PLB to OPB bridge core features:

- PLB slave device and OPB master device
- External programmable address space via address decode pin (this allows the PLB-to-OPB Bridge to be located anywhere in the address map.
- Supports 8 PLB masters
- 64-bit PLB slave interface supports
 - Double Word (64-bit) writes or (32-bit writes) and Word (32-bit) reads
 - All partial transfers (see PLB architecture)
- Supports word, halfword, and byte burst reads and writes, including fixed-length bursts
- Supports pipelining for read transfers
- Compliant with quad-, and octal-word bursts for upward compatibility
- Supports 4-, 8-, and 16-word line transfers
- Line reads performed target-word-first for minimum latency
- OPB master performs dynamic bus sizing for varying width slave devices
- Bus error log accessible through device control registers
- 50+ MHz OPB clock frequency
- Support for PLB bus-speeds at 1x, 2x, 3x, or 4x the frequency of the OPB
- Support for clock and class II power management
- Two deep word write data buffers with steering and replication logic, dynamically configurable as a single doubleword buffer or two individual word buffers.
- Three deep FIFO structure for reads and writes. Will accept either two read requests or two write requests from the PLB in any order; however will not accept three writes or three reads at the same time.
- Word read data buffer, supporting data packing from OPB slaves
- Watchdog timer for implementations omitting OPB arbiter

Who Should Use This Book

This book is for hardware, software, and application developers who need to understand system-on-a-chip (SOC) designs. The audience should understand embedded system design, operating systems, and the principles of computer organization.

Chapter 1. PLB to OPB Bridge Overview

The processor local bus (PLB) to on-chip peripheral bus (OPB) bridge is a soft core which enables transfers of data between the PLB and OPB under the direction of PLB master devices. The bridge is a slave on the PLB and a master on the OPB. The bridge is necessary in any system implementation with OPB slave devices, which must be accessed by the processor.

Features of the PLB to OPB bridge include:

- PLB slave device and OPB master device
- External programmable address space via address decode pin (this allows the PLB to OPB Bridge to be located anywhere in the address map.
- Supports 8 PLB masters
- 64-bit PLB slave interface supports
 - Double Word (64-bit) writes or (32-bit writes) and Word (32-bit) reads
 - All partial transfers (see PLB architecture)
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- Two deep word write data buffers with steering and replication logic, dynamically configurable as a single doubleword buffer or two individual word buffers.
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- Watchdog timer for implementations omitting OPB arbiter

Figure 1 demonstrates how the PLB to OPB bridge is inter connected for the purpose of system-on-a-chip design.

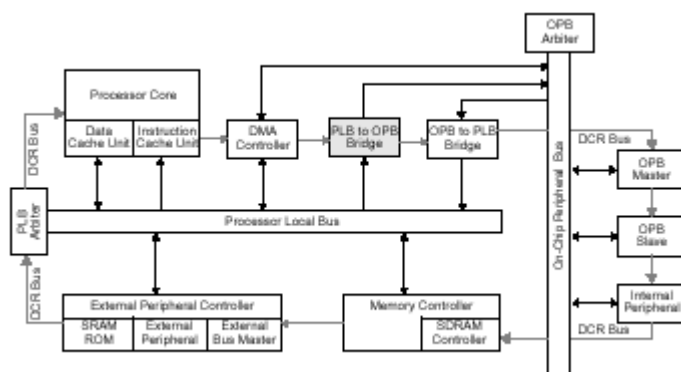


Figure 1. PLB to OPB Bridge Interconnection

As shown in Figure 1, the on-chip bus structure provides a link between the processor core and other peripherals which consist of PLB and OPB master and slave devices.

The processor local bus (PLB) is the high performance bus used to access memory through the bus interface units. The two bus interface units shown above: external peripheral controller and memory controller are the PLB slaves. The processor core has two PLB master connections, one for instruction cache and one for data cache. Attached to the PLB is also the direct memory access (DMA) controller, which is a PLB master device used in data intensive applications to improve data transfer performance.

Lower performance peripherals (such as OPB master, slave, and other internal peripherals) are attached to the on-chip peripheral bus (OPB). A bridge is provided between the PLB and OPB to enable data transfer by PLB masters to and from OPB slaves. In the above example we have two bridges, a PLB to OPB bridge which is a slave on the PLB and a master on the OPB and an OPB to PLB bridge which is a slave on the OPB and a master on the PLB. OPB peripherals may also comprise DMA peripherals.

The device control register (DCR) bus is used primarily for accessing status and control registers within the various PLB and OPB masters and slaves. It is meant to off-load the PLB from the lower performance status and control read and write transfers. The DCR bus architecture allows data transfers among OPB peripherals to occur independently from, and concurrent with, data transfers between the processor and memory, or among other PLB devices.

Figure 2 provides a block diagram of the PLB to OPB bridge.

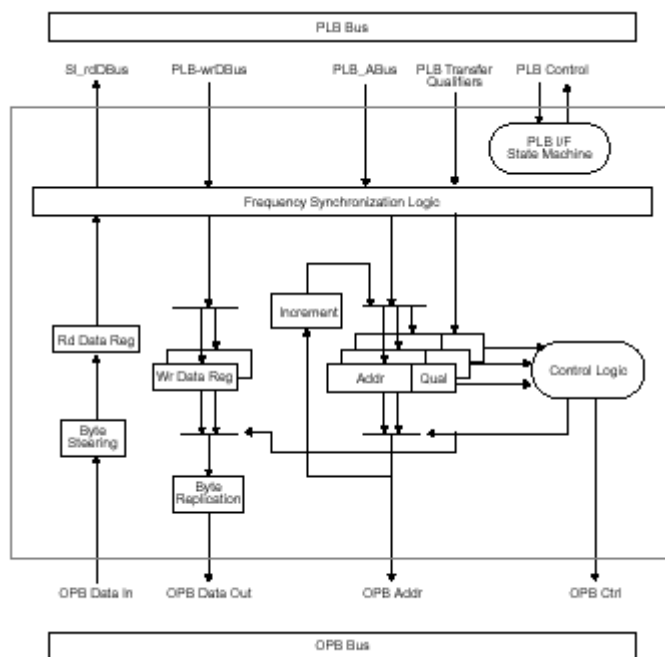


Figure 2. PLB to OPB Bridge Core Block Diagram

1.1 PLB Interface

The PLB to OPB bridge interfaces to the PLB as a 64-bit slave device for write operations, and as a 32-bit slave for reads. It has a single input for address decode so that the OPB slaves may be relocated in the system address map.

The PLB to OPB bridge has several features that enhance its ability to decrease latency on the PLB bus. These are:

- The PLB interface supports secondary read acknowledgments, allowing the bridge to access data from an OPB slave while a current PLB read operation is pending or in process. This will reduce latency in providing the PLB master with the data when the request becomes a primary read

request.

- Also to reduce PLB bus latency, the PLB to OPB bridge will accept posted writes – latching address, qualifiers, and write data from the PLB - and then accept subsequent PLB transfers before completing the write to the OPB slave. This frees the PLB write bus for other masters. Two such posted writes may be accepted if they are not both burst or line writes.
- The PLB to OPB bridge contains logic which steps down the PLB frequency by an integer amount (2:1, 3:1, etc.), allowing the OPB side of the bridge to run at the same (slower) frequency as the OPB. The PLB side always runs at the PLB bus frequency.

All PLB to OPB bridge operations on the OPB are performed in the order accepted by the PLB. This insures that coherency is preserved.

1.2 PLB to OPB Bridge Buffering

The PLB to OPB bridge buffering section discusses data buffering, address and transfer qualifiers buffering and error registers.

1.2.1 Data Buffering

The PLB to OPB bridge contains an 8 byte write data buffer, dynamically configurable as a single 64-bit, or two independent 32-bit data registers, and a separate 4 byte read data register. The write buffer resources are dynamically configured to the width of the requested write data transfer. If for example a 64 partial word write is requested that only uses the upper or lower word, then the PLB to OPB bridge will respond as a 64-bit device but will only use one write buffer keeping the other one free for another 32-bit or 64-bit write request.

1.2.2 Address and Transfer Qualifiers Buffering

The PLB to OPB bridge contains three sets of address and PLB transfer qualifier registers. These FIFO address and qualifier registers are dynamically allocated between reads and writes. The PLB to OPB bridge may accept a secondary read request or a second primary write request, depending on the current allocation of data buffer resources and the state of the current transfer. The following rules (on how PLB requests are accepted) are in order:

- At most, only two reads or two writes can be accepted at any one time. If, say two reads have been accepted then only one write can be accepted and similarly if two writes have been accepted, then only one read can be accepted.
- If a 64-bit word write is accepted, and the master is requesting more than four bytes of data and the PLB to OPB bridge responds back as a 64-bit slave device then both write buffers are in use and the PLB to OPB bridge will not addrAck another write until the lower word, or bytes of the lower word, have been written.
- 64-bit word write requests that either only use the upper or lower word, (that is, 4 bytes or less confined to either the upper or lower word) will be answered as a 64 slave write and will only use one write buffer, thus the PLB to OPB bridge will be able to accept another write request.
- Write line or burst requests once addrAcked will prevent further PLB write requests from being addrAcked until the current line write or burst write is completed. The PLB to OPB bridge only accepts primary writes.
- Read line or burst requests once addrAcked will still allow a secondary request to be accepted if there is a free position in the address queue.
- 64-bit read requests are always accepted with the PLB to OPB bridge responding as a 32-bit slave device.
- If the PLB to OPB bridge has an open write buffer and a 64-bit write request comes in with data in both the upper and lower words then the PLB to OPB bridge will always accept the requests and

respond as a 32-bit slave device necessitating a conversion cycle by the master.

- The PLB to OPB bridge always responds as a 32-bit slave device for line and burst writes and for all read accesses.
- Write bursts of 1 are treated like word request as far as the FIFO is concerned. Thus they will not stall the PLB to OPB bridge from accepting the next write requests until the end of the write on the OPB.

1.2.3 Error Registers

The PLB to OPB bridge also contains a set of error reporting registers accessed through the device control register (DCR) bus. There are two 32-bit registers, one for the address that the error occurred at - Bridge Error Address Register (GEAR), and one that contains what type of error occurred and for which master - Bridge Error Status Register (GESR). The GESR is broken up into 8 fields, one for each of the eight masters supported.

1.3 OPB Interface

The PLB to OPB bridge interfaces to the OPB as a 32-bit master device. It fully implements the OPB architecture, performing dynamic bus sizing transfers as necessary. The OPB timeout counter, normally contained in the OPB arbiter, is replicated in the PLB to OPB bridge. This allows for efficient implementation of system designs with only slave devices attached to the OPB. In this case, the PLB to OPB bridge is the only master device on the OPB, and the arbiter need not be attached.

1.4 Address Registers

Separate 32-bit PLB addresses are registered by the PLB to OPB bridge for each operation. Byte addresses are incremented as necessary to implement dynamic bus sizing on the OPB. Word addresses are incremented only for PLB burst and line transfers. All line transfers are performed target word first for minimum latency. The PLB to OPB bridge address incrementer tracks the requested line size, and wraps the line address appropriately.

1.5 Error Logging and Reporting

OPB errors (timeout and slave error acknowledge) are logged and reported to the requesting PLB master in conformance to the PLB architecture. The error logging registers can be accessed by using the DCR bus.

1.6 Watchdog Timer

The OPB watchdog timer generates timeout errors for all OPB master devices. A timeout counter in the PLB to OPB bridge is enabled to support system implementations where the PLB to OPB bridge is the only OPB master device. This counter monitors only the response delay of the OPB slave devices addressed by the PLB to OPB bridge, and should be disabled when the PLB to OPB bridge is used in a multi-master OPB implementation.

If the PLB to OPB bridge initiates an OPB transfer and does not receive a valid acknowledgement within sixteen cycles, and the addressed slave device does not assert its time-out suppress signal within the sixteen cycles, the watchdog timer will assert a timeout signal to the PLB to OPB bridge error logging and reporting registers. For additional information on timeout and timeout suppression refer to the OPB architecture.

The internal timeout and the OPB_timeout input signal are logically ORed together.

1.7 Clock and Power Management

Power consumption within the PLB to OPB bridge is reduced by gating the clock to all latches internally. Minimum power is achieved when no active PLB requests are pending and the OPB is idle.

In addition, a sleep request signal is provided to be used by a central clock and power management unit in a system. This signal is asserted by the PLB to OPB bridge to indicate when it is permissible to shut-off its clocks. There are two clock power management units residing in the core, one each for the PLB clock and OPB clock. These clock power management units gracefully shut off the clocks to the individual latches by gating the clock splitter. They also correctly sync up the restart of the clocks.

Chapter 2. PLB to OPB Bridge Registers

From a programming perspective, there are three accessible device control registers residing in the PLB to OPB bridge: Bridge Error Address Register (GEAR), Bridge Error Status Register 0 (GESR0), Bridge Error Status Register 1 (GESR1). Figure 7 provides a summary of all PLB to OPB bridge registers which are discussed in detail in this section.

Figure 7. PLB to OPB Bridge Registers

Mnemonic	Register Name	Decode	Access
GEAR	Bridge Error Address Register	0x0B2	Read Only
GESR0	Bridge Error Status Register 0 Master Devices 0,1,2,3	0x0B0	Read/Clear
GESR1	Bridge Error Status Register Master Devices 4,5,6,7	0x0B4	Read/Clear

2.1 Bridge Error Address Register (GEAR)

The Bridge Error Address Register (GEAR) is a read-only register. As part of its error reporting, the PLB to OPB bridge will load the GEAR with the error address if the ALCK, (address lock bit), is not already set. If the master's Mn_lockError signal was asserted when the PLB to OPB bridge accepted the PLB transfer, the GEAR will lock, (if the ALCK bit is not already set either by this master or another master), upon loading the first error address (the master's ALCK bit is set in the GESRn).

Once locked, the GEAR cannot be overwritten until all the GESRn address locking bits, (total of eight, one for each master), are cleared by using the move to device control register (**mtdcr**) instruction.

Figure 8 shows bit definitions for GEAR.

Note: To reiterate a point in the above paragraph. Any master that asserts Mn_lockError will lock the GEAR and this will prevent anymore updates to the GEAR by any master, including the locking master until software clears the ALCK lock bits out.

DCR Read Address = 0x0B2.

0	31
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Figure 8. Bridge Error Address Register (GEAR)

0:31	0x0B2	Address of bus error
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2.2 Bridge Error Status Registers (GESRn)

In addition to driving the current PLB master's error input signal, (PLB_MnErr), the PLB to OPB bridge will also record the error information into the appropriate master's Bridge Error Status Register (GESRn) field (provided that the register is not already locked by a previous error that also was locked), where it could be optionally locked by the master having its Mn_lockErr signal asserted at the time the PLB to OPB bridge accepted the PLB operation.

Once locked, a master's GESRn field cannot be overwritten if any subsequent error occurs, until cleared by using the move to device control register (**mtdcr**) instruction. To clear either GESRn, a "1" must be loaded into those register bits that are to be cleared using the proper DCR access address.

Writing a "0" to any bit in either GESRn will not affect the status of that bit.

The PLB to OPB Bridge contains two GESR's: Bridge Error Status Register 0 (GESR0) logs error data for PLB masters 0-3, and Bridge Error Status Register 1 (GESR1) logs error data for PLB masters 4-7.

Table 10 lists the GESRn registers and their DCR access addresses for reading, clearing and setting

the various bits followed by GESR0 and GESR1 bit definitions.

Table 10. DCR Register Addresses

Neumonic	Description	Masters Logged	DCR Address
GESR0	Read/Clear Address	0, 1, 2, 3	0x0B0
GESR0	Write/Set Address	0, 1, 2, 3	0x0B1
GESR1	Read/Clear Address	4, 5, 6, 7	0x0B4
GESR1	Write/Set Address	4, 5, 6, 7	0x0B5

2.2.1 Bridge Error Status Register 0 (GESR0)

Figure 9 shows bit definitions for GESR0.



Figure 9. Bridge Error Status Register 0 (GESR0)

0:1	PTE0	PLB timeout error status master 0 00 No master 0 error occurred 01 Master 0 timeout error occurred 10 Master 0 slave error occurred 11 Reserved
2	R/W0	Read write status master 0 0 Master 0 error operation is a read 1 Master 0 error operation is a write
3	FLK0	GESR field lock master 0 0 Master 0 GESR field is unlocked 1 Master 0 GESR field is locked
4	ALK0	GEAR address lock master 0 0 Master 0 GEAR address is unlocked 1 Master 0 GEAR address is locked
5:6	PTE1	PLB timeout error status master 1 00 No master 1 error occurred 01 Master 1 timeout error occurred 10 Master 1 slave error occurred 11 Reserved
7	R/W1	Read/write status master 1 0 Master 1 error operation is a read 1 Master 1 error operation is a write
8	FLK1	GESR field lock master 1 0 Master 1 GESR field is unlocked 1 Master 1 GESR field is locked
9	ALK1	GEAR address lock master 1 0 Master 1 GEAR address is unlocked 1 Master 1 GEAR address is locked
10:11	PTE2	PLB timeout error status master 2 00 No master 2 error occurred 01 Master 2 timeout error occurred 10 Master 2 slave error occurred 11 Reserved
12	R/W2	Read/write status master 2 0 Master 2 error operation is a read 1 Master 2 error operation is a write
13	FLK2	GESR field lock master 2 0 Master 2 GESR field is unlocked 1 Master 2 GESR field is locked
14	ALK2	GEAR address lock master 2 0 Master 2 GEAR address is unlocked 1 Master 2 GEAR address is locked

15:16	PTE3	PLB timeout error status master 3 00 No master 3 error occurred 01 Master 3 timeout error occurred 10 Master 3 slave error occurred 11 Reserved
17	R/W3	Read/write status master 3 0 Master 3 error operation is a read 1 Master 3 error operation is a write
18	FLK3	GESR field lock master 3 0 Master 3 GESR field is unlocked 1 Master 3 GESR field is locked
19	ALK3	GEAR address lock master 3 0 Master 3 GEAR address is unlocked 1 Master 3 GEAR address is locked
20:31		Reserved

2.2.2 Bridge Error Status Register 1 (GESR1)

Figure 10 shows bit definitions for GESR1.

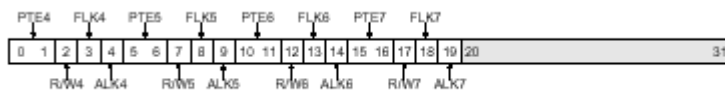


Figure 10. Bridge Error Status Register 1 (GESR1)

0:1	PTE4	PLB timeout error status Master 4 00 No Master 4 error occurred 01 Master 4 timeout error occurred 10 Master 4 slave error occurred 11 Reserved
2	R/W4	Read write status Master 4 0 Master 4 error operation is a read 1 Master 4 error operation is a write
3	FLK4	GESR field lock Master 1 0 Master 4 GESR field is unlocked 1 Master 4 GESR field is locked
4	ALK4	GEAR address lock Master 4 0 Master 4 GEAR address is unlocked 1 Master 4 GEAR address is locked
5:6	PTE5	PLB timeout error status Master 5 00 No Master 5 error occurred 01 Master 5 timeout error occurred 10 Master 5 slave error occurred 11 Reserved
7	R/W5	Read/write status Master 5 0 Master 5 error operation is a read 1 Master 5 error operation is a write
8	FLK5	GESR field lock Master 5 0 Master 5 GESR field is unlocked 1 Master 5 GESR field is locked
9	ALK5	GEAR address lock Master 5 0 Master 5 GEAR address is unlocked 1 Master 5 GEAR address is locked
10:11	PTE6	PLB timeout error status Master 6 00 No Master 6 error occurred 01 Master 6 timeout error occurred 10 Master 6 slave error occurred 11 Reserved
12	R/W6	Read/write status Master 6 0 Master 6 error operation is a read 1 Master 6 error operation is a write

13	FLK6	GESR field lock Master 6 0 Master 6 GESR field is unlocked 1 Master 6 GESR field is locked
14	ALK6	GEAR address lock Master 6 0 Master 6 GEAR address is unlocked 1 Master 6 GEAR address is locked
15:16	PTE7	PLB timeout error status Master 7 00 No Master 7 error occurred 01 Master 7 timeout error occurred 10 Master 7 slave error occurred 11 Reserved
17	R/W7	Read/write status Master 7 0 Master 7 error operation is a read 1 Master 7 error operation is a write
18	FLK7	GESR field lock Master 7 0 Master 7 GESR field is unlocked 1 Master 7 GESR field is locked
19	ALK7	GEAR address lock Master 7 0 Master 7 GEAR address is unlocked 1 Master 7 GEAR address is locked
20:31		Reserved



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