

LC77700B

(PowerPC 405IAP Embedded Processor)

User's Manual

GPIO

Connections

(General Purpose I/O Controller)

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1. GPIO Grouping

Below table shows main functions of GPIO groups.

GPIO Group	Grouping IP Name	GPIO Number/IP	Total Number
GPIO0	LCDC	32	32
GPIO1	KeyScan	28	32
	EBC	2	
	PS2	2	
GPIO2	PCMCIA	20	32
	UIC	8	
	IrDA	4	
GPIO3	UART1 IOM2 HDLC0	14	32
	SCI	5	
	TPC	5	
	UART0	8	
GPIO4	IEEE1284	18	27
	Trace	9	
	Rest	5	

2. Signal Assignment

notation : ex GPIOX_Y_TS_control, GPIOX_Y_Out, GPIOX_Y_In
X : GPIO Number, Y : Bit assignment

2.1. GPIO0

GPIO Signals	Bit0	Bit1	Bit2	Bit3
Alt_Output_1	FPDATA0	FPDATA1	FPDATA2	FPDATA3
Alt_Output_2	Low	Low	Low	Low
Alt_Output_3	Low	Low	Low	Low
Alt_TS_Control_1	High	High	High	High
Alt_TS_Control_2	Low	Low	Low	Low
Alt_TS_Control_3	Low	Low	Low	Low
Alt_Receive_1	Low	Low	Low	Low
Alt_Receive_2	Low	Low	Low	Low
Alt_Receive_3	Low	Low	Low	Low
Alt_Input_1	Open	Open	Open	Open
Alt_Input_2	Open	Open	Open	Open
Alt_Input_3	Open	Open	Open	Open
GPIO_TS_control	GPIO0_0_TS_control	GPIO0_1_TS_control	GPIO0_2_TS_control	GPIO0_3_TS_control
GPIO_Out	GPIO0_0_Out	GPIO0_1_Out	GPIO0_2_Out	GPIO0_3_Out
GPIO_In	GPIO0_0_In	GPIO0_1_In	GPIO0_2_In	GPIO0_3_In
Pad Signals				
Module Pin Name	LCDD0	LCDD1	LCDD2	LCDD3

GPIO Signals	Bit4	Bit5	Bit6	Bit7
Alt_Output_1	FPDATA4	FPDATA5	FPDATA6	FPDATA7
Alt_Output_2	Low	Low	Low	Low
Alt_Output_3	Low	Low	Low	Low
Alt_TS_Control_1	High	High	High	High
Alt_TS_Control_2	Low	Low	Low	Low
Alt_TS_Control_3	Low	Low	Low	Low
Alt_Receive_1	Low	Low	Low	Low
Alt_Receive_2	Low	Low	Low	Low
Alt_Receive_3	Low	Low	Low	Low
Alt_Input_1	Open	Open	Open	Open
Alt_Input_2	Open	Open	Open	Open
Alt_Input_3	Open	Open	Open	Open
GPIO_TS_control	GPIO0_4_TS_control	GPIO0_5_TS_control	GPIO0_6_TS_control	GPIO0_7_TS_control
GPIO_Out	GPIO0_4_Out	GPIO0_5_Out	GPIO0_6_Out	GPIO0_7_Out
GPIO_In	GPIO0_4_In	GPIO0_5_In	GPIO0_6_In	GPIO0_7_In
Pad Signals				
Module Pin Name	LCDD4	LCDD5	LCDD6	LCDD7

GPIO Signals	Bit8	Bit9	Bit10	Bit11
Alt_Output_1	FPDATA8	FPDATA9	FPDATA10	FPDATA11
Alt_Output_2	Low	Low	Low	Low
Alt_Output_3	Low	Low	Low	Low
Alt_TS_Control_1	High	High	High	High
Alt_TS_Control_2	Low	Low	Low	Low
Alt_TS_Control_3	Low	Low	Low	Low
Alt_Receive_1	Low	Low	Low	Low
Alt_Receive_2	Low	Low	Low	Low
Alt_Receive_3	Low	Low	Low	Low
Alt_Input_1	Open	Open	Open	Open
Alt_Input_2	Open	Open	Open	Open
Alt_Input_3	Open	Open	Open	Open
GPIO_TS_control	GPIO0_8_TS_control	GPIO0_9_TS_control	GPIO0_10_TS_control	GPIO0_11_TS_control
GPIO_Out	GPIO0_8_Out	GPIO0_9_Out	GPIO0_10_Out	GPIO0_11_Out
GPIO_In	GPIO0_8_In	GPIO0_9_In	GPIO0_10_In	GPIO0_11_In
Pad Signals				
Module Pin Name	LCDD8	LCDD9	LCDD10	LCDD11

GPIO Signals	Bit12	Bit13	Bit14	Bit15
Alt_Output_1	FPDATA12	FPDATA13	FPDATA14	FPDATA15

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Alt_Output_2	Low	Low	Low	Low
Alt_Output_3	Low	Low	Low	Low
Alt_TS_Control_1	High	High	High	High
Alt_TS_Control_2	Low	Low	Low	Low
Alt_TS_Control_3	Low	Low	Low	Low
Alt_Receive_1	Low	Low	Low	Low
Alt_Receive_2	Low	Low	Low	Low
Alt_Receive_3	Low	Low	Low	Low
Alt_Input_1	Open	Open	Open	Open
Alt_Input_2	Open	Open	Open	Open
Alt_Input_3	Open	Open	Open	Open
GPIO_TS_control	GPIO0_12_TS_control	GPIO0_13_TS_control	GPIO0_14_TS_control	GPIO0_15_TS_control
GPIO_Out	GPIO0_12_Out	GPIO0_13_Out	GPIO0_14_Out	GPIO0_15_Out
GPIO_In	GPIO0_12_In	GPIO0_13_In	GPIO0_14_In	GPIO0_15_In
Pad Signals				
Module Pin Name	LCDD12	LCDD13	LCDD14	LCDD15

GPIO Signals	Bit16	Bit17	Bit18	Bit19
Alt_Output_1	FPDATA16	FPDATA17	FPDATA18	FPDATA19
Alt_Output_2	PCIC_RESET1	Low	Low	Low
Alt_Output_3	Low	Low	Low	Low
Alt_TS_Control_1	High	High	High	High
Alt_TS_Control_2	High	Low	Low	Low
Alt_TS_Control_3	Low	Low	Low	Low
Alt_Receive_1	Low	Low	Low	Low
Alt_Receive_2	Low	Low	Low	Low
Alt_Receive_3	Low	Low	Low	Low
Alt_Input_1	Open	Open	Open	Open
Alt_Input_2	Open	Open	Open	Open
Alt_Input_3	Open	Open	Open	Open
GPIO_TS_control	GPIO0_16_TS_control	GPIO0_17_TS_control	GPIO0_18_TS_control	GPIO0_19_TS_control
GPIO_Out	GPIO0_16_Out	GPIO0_17_Out	GPIO0_18_Out	GPIO0_19_Out
GPIO_In	GPIO0_16_In	GPIO0_17_In (PCIC_CD11B)	GPIO0_18_In (PCIC_CD12B)	GPIO0_19_In (PCIC_VS11B)
Pad Signals				
Module Pin Name	LCDD16	LCDD17	LCDD18	LCDD19

GPIO Signals	Bit20	Bit21	Bit22	Bit23
Alt_Output_1	FPDATA20	FPDATA21	FPDATA22	FPDATA23
Alt_Output_2	Low	Low	Low	Low
Alt_Output_3	Low	Low	Low	Low
Alt_TS_Control_1	High	High	High	High
Alt_TS_Control_2	Low	Low	Low	Low
Alt_TS_Control_3	Low	Low	Low	Low
Alt_Receive_1	Low	Low	Low	Low
Alt_Receive_2	Low	Low	Low	Low
Alt_Receive_3	Low	Low	Low	Low
Alt_Input_1	Open	Open	Open	Open
Alt_Input_2	Open	Open	Open	Open
Alt_Input_3	Open	Open	Open	Open
GPIO_TS_control	GPIO0_20_TS_control	GPIO0_21_TS_control	GPIO0_22_TS_control	GPIO0_23_TS_control
GPIO_Out	GPIO0_20_Out	GPIO0_21_Out	GPIO0_22_Out	GPIO0_23_Out
GPIO_In	GPIO0_20_In (PCIC_VS12B)	GPIO0_21_In (PCIC_BVD11B)	GPIO0_22_In (PCIC_BVD12B)	GPIO0_23_In (PCIC_WP1B)
Pad Signals				
Module Pin Name	LCDD20	LCDD21	LCDD22	LCDD23

GPIO Signals	Bit24	Bit925	Bit26	Bit27
Alt_Output_1	Low	FP_EN	FP_VEE_EN	FP_VDD_EN
Alt_Output_2	Low	Low	Low	Low
Alt_Output_3	Low	Low	Low	Low
Alt_TS_Control_1	Low	High	High	High
Alt_TS_Control_2	Low	Low	Low	Low
Alt_TS_Control_3	Low	Low	Low	Low

Alt_Receive_1	Low	Low	Low	Low
Alt_Receive_2	Low	Low	Low	Low
Alt_Receive_3	Low	Low	Low	Low
Alt_Input_1	Open	Open	Open	Open
Alt_Input_2	Open	Open	Open	Open
Alt_Input_3	Open	Open	Open	Open
GPIO_TS_control	GPIO0_24_TS_control	GPIO0_25_TS_control	GPIO0_26_TS_control	GPIO0_27_TS_control
GPIO_Out	GPIO0_24_Out	GPIO0_25_Out	GPIO0_26_Out	GPIO0_27_Out
GPIO_In	GPIO0_24_In (Lcd_Reset_N)	GPIO0_25_In	GPIO0_26_In	GPIO0_27_In
Pad Signals				
Module Pin Name	LCDRSTN	LCDEN	LCDVEEEN	LCDVDDEN

GPIO Signals	Bit28	Bit29	Bit30	Bit31
Alt_Output_1	FP_MUX	FPSHIFT	FPLINE	FPFRAME
Alt_Output_2	Low	Low	Low	Low
Alt_Output_3	Low	Low	Low	Low
Alt_TS_Control_1	High	High	High	High
Alt_TS_Control_2	Low	Low	Low	Low
Alt_TS_Control_3	Low	Low	Low	Low
Alt_Receive_1	Low	Low	Low	Low
Alt_Receive_2	Low	Low	Low	Low
Alt_Receive_3	Low	Low	Low	Low
Alt_Input_1	Open	Open	Open	Open
Alt_Input_2	Open	Open	Open	Open
Alt_Input_3	Open	Open	Open	Open
GPIO_TS_control	GPIO0_28_TS_control	GPIO0_29_TS_control	GPIO0_30_TS_control	GPIO0_31_TS_control
GPIO_Out	GPIO0_28_Out	GPIO0_29_Out	GPIO0_30_Out	GPIO0_31_Out
GPIO_In	GPIO0_28_In	GPIO0_29_In	GPIO0_30_In	GPIO0_31_In
Pad Signals				
Module Pin Name	LCDMUX	LCDSHFT	LCDLINE	LCDFRM

2.2. GPIO1

GPIO Signals	Bit0	Bit1	Bit2	Bit3
Alt_Output_1	Low	Low	Low	Low
Alt_Output_2	ROW640	ROW641	ROW642	ROW643
Alt_Output_3	Low	Low	Low	Low
Alt_TS_Control_1	High	High	High	High
Alt_TS_Control_2	High	High	High	High
Alt_TS_Control_3	Low	Low	Low	Low
Alt_Receive_1	Low	Low	Low	Low
Alt_Receive_2	Low	Low	Low	Low
Alt_Receive_3	Low	Low	Low	Low
Alt_Input_1	Open	Open	Open	Open
Alt_Input_2	Open	Open	Open	Open
Alt_Input_3	Open	Open	Open	Open
GPIO_TS_control	GPIO1_0_TS_control	GPIO1_1_TS_control	GPIO1_2_TS_control	GPIO1_3_TS_control
GPIO_Out	GPIO1_0_Out	GPIO1_1_Out	GPIO1_2_Out	GPIO1_3_Out
GPIO_In	GPIO1_0_In	GPIO1_1_In	GPIO1_2_In	GPIO1_3_In
Pad Signals				
Module Pin Name	KOUT0N	KOUT1N	KOUT2N	KOUT3N

GPIO Signals	Bit4	Bit5	Bit6	Bit7
Alt_Output_1	Low	Low	Low	Low
Alt_Output_2	ROW644	ROW645	Low	Low
Alt_Output_3	Low	Low	Low	Low
Alt_TS_Control_1	High	High	High	High
Alt_TS_Control_2	High	High	Low	Low
Alt_TS_Control_3	Low	Low	Low	Low
Alt_Receive_1	Low	Low	Low	Low
Alt_Receive_2	Low	Low	Low	Low
Alt_Receive_3	Low	Low	Low	Low
Alt_Input_1	Open	Open	Open	Open
Alt_Input_2	Open	Open	Open	Open
Alt_Input_3	Open	Open	Open	Open
GPIO_TS_control	GPIO1_4_TS_control	GPIO1_5_TS_control	GPIO1_6_TS_control	GPIO1_7_TS_control
GPIO_Out	GPIO1_4_Out	GPIO1_5_Out	GPIO1_6_Out	GPIO1_7_Out
GPIO_In	GPIO1_4_In	GPIO1_5_In	GPIO1_6_In	GPIO1_7_In
Pad Signals				
Module Pin Name	KOUT4N	KOUT5N	KOUT6N	KOUT7N

GPIO Signals	Bit8	Bit9	Bit10	Bit11
Alt_Output_1	Low	Low	Low	Low
Alt_Output_2	Low	Low	Low	Low
Alt_Output_3	Low	Low	Low	Low
Alt_TS_Control_1	High	High	High	High
Alt_TS_Control_2	Low	Low	Low	Low
Alt_TS_Control_3	Low	Low	Low	Low
Alt_Receive_1	Low	Low	Low	Low
Alt_Receive_2	Low	Low	Low	Low
Alt_Receive_3	Low	Low	Low	Low
Alt_Input_1	Open	Open	Open	Open
Alt_Input_2	Open	Open	Open	Open
Alt_Input_3	Open	Open	Open	Open
GPIO_TS_control	GPIO1_8_TS_control	GPIO1_9_TS_control	GPIO1_10_TS_control	GPIO1_11_TS_control
GPIO_Out	GPIO1_8_Out	GPIO1_9_Out	GPIO1_10_Out	GPIO1_11_Out
GPIO_In	GPIO1_8_In	GPIO1_9_In	GPIO1_10_In	GPIO1_11_In
Pad Signals				
Module Pin Name	KOUT8N	KOUT9N	KOUT10N	KOUT11N

GPIO Signals	Bit12	Bit13	Bit14	Bit15
Alt_Output_1	Low	Low	Low	Low
Alt_Output_2	Low	Low	Low	SC_DTSC
Alt_Output_3	Low	Low	Low	Low
Alt_TS_Control_1	High	High	High	High

Alt_TS_Control_2	Low	Low	Low	High
Alt_TS_Control_3	Low	Low	Low	Low
Alt_Receive_1	Low	Low	GPIO2_27_In	Low
Alt_Receive_2	Low	Low	Low	Low
Alt_Receive_3	Low	Low	Low	Low
Alt_Input_1	Open	Open	In_interrupt7	Open
Alt_Input_2	Open	Open	Open	Open
Alt_Input_3	Open	Open	Open	Open
GPIO_TS_control	GPIO1_12_TS_control	GPIO1_13_TS_control	GPIO1_14_TS_control	GPIO1_15_TS_control
GPIO_Out	GPIO1_12_Out	GPIO1_13_Out	GPIO1_14_Out	GPIO1_15_Out
GPIO_In	GPIO1_12_In	GPIO1_13_In	GPIO1_14_In	GPIO1_15_In
Pad Signals				
Module Pin Name	KOUT12N	KOUT13N	KOUT14N	KOUT15N

GPIO Signals	Bit16	Bit17	Bit18	Bit19
Alt_Output_1	Low	Low	Low	Low
Alt_Output_2	Low	Low	Low	Low
Alt_Output_3	Low	Low	Low	Low
Alt_TS_Control_1	Low	Low	Low	Low
Alt_TS_Control_2	Low	Low	Low	Low
Alt_TS_Control_3	Low	Low	Low	Low
Alt_Receive_1	Low	Low	Low	Low
Alt_Receive_2	Low	Low	Low	Low
Alt_Receive_3	Low	Low	Low	Low
Alt_Input_1	Open	Open	Open	Open
Alt_Input_2	Open	Open	Open	Open
Alt_Input_3	Open	Open	Open	Open
GPIO_TS_control	GPIO1_16_TS_control	GPIO1_17_TS_control	GPIO1_18_TS_control	GPIO1_19_TS_control
GPIO_Out	GPIO1_16_Out	GPIO1_17_Out	GPIO1_18_Out	GPIO1_19_Out
GPIO_In	GPIO1_16_In (COL0, COL640)	GPIO1_17_In (COL1, COL641)	GPIO1_18_In (COL2, COL642)	GPIO1_19_In (COL3, COL643)
Pad Signals				
Module Pin Name	KIN0N	KIN1N	KIN2N	KIN3N

GPIO Signals	Bit20	Bit21	Bit22	Bit23
Alt_Output_1	Low	Low	Low	Low
Alt_Output_2	Low	Low	Low	Low
Alt_Output_3	Low	Low	Low	Low
Alt_TS_Control_1	Low	Low	Low	Low
Alt_TS_Control_2	Low	Low	Low	Low
Alt_TS_Control_3	Low	Low	Low	Low
Alt_Receive_1	Low	Low	Low	Low
Alt_Receive_2	Low	Low	Low	Low
Alt_Receive_3	Low	Low	Low	Low
Alt_Input_1	Open	Open	Open	Open
Alt_Input_2	Open	Open	Open	Open
Alt_Input_3	Open	Open	Open	Open
GPIO_TS_control	GPIO1_20_TS_control	GPIO1_21_TS_control	GPIO1_22_TS_control	GPIO1_23_TS_control
GPIO_Out	GPIO1_20_Out	GPIO1_21_Out	GPIO1_22_Out	GPIO1_23_Out
GPIO_In	GPIO1_20_In (COL4)	GPIO1_21_In (COL5)	GPIO1_22_In (COL6)	GPIO1_23_In (COL7)
Pad Signals				
Module Pin Name	KIN4N	KIN5N	KIN6N	KIN7N

GPIO Signals	Bit24	Bit25	Bit26	Bit27
Alt_Output_1	Low	Low	Low	Low
Alt_Output_2	Low	Low	Low	Low
Alt_Output_3	Low	Low	Low	Low
Alt_TS_Control_1	Low	Low	Low	Low
Alt_TS_Control_2	Low	Low	Low	Low
Alt_TS_Control_3	Low	Low	Low	Low
Alt_Receive_1	Low	Low	Low	Low
Alt_Receive_2	Low	Low	Low	Low
Alt_Receive_3	Low	Low	Low	Low

Alt_Input_1	Open	Open	Open	Open
Alt_Input_2	Open	Open	Open	Open
Alt_Input_3	Open	Open	Open	Open
GPIO_TS_control	GPIO1_24_TS_control	GPIO1_25_TS_control	GPIO1_26_TS_control	GPIO1_27_TS_control
GPIO_Out	GPIO1_24_Out	GPIO1_25_Out	GPIO1_26_Out	GPIO1_27_Out
GPIO_In	GPIO1_24_In (COL8)	GPIO1_25_In (COL9)	GPIO1_26_In (COL10)	GPIO1_27_In (COL11)
Pad Signals				
Module Pin Name	KIN8N	KIN9N	KIN10N	KIN11N

GPIO Signals	Bit28	Bit29	Bit30	Bit31
Alt_Output_1	EPC_Addr6	EPC_Addr7	PS2Clockout	PS2Dataout
Alt_Output_2	Low	Low	Low	Low
Alt_Output_3	Low	Low	Low	Low
Alt_TS_Control_1	High	High	PS2Clocken	PS2Dataen
Alt_TS_Control_2	Low	Low	Low	Low
Alt_TS_Control_3	Low	Low	Low	Low
Alt_Receive_1	Low	Low	Low	Low
Alt_Receive_2	Low	Low	Low	Low
Alt_Receive_3	Low	Low	Low	Low
Alt_Input_1	Open	Open	Open	Open
Alt_Input_2	Open	Open	Open	Open
Alt_Input_3	Open	Open	Open	Open
GPIO_TS_control	GPIO1_28_TS_control	GPIO1_29_TS_control	GPIO1_30_TS_control	GPIO1_31_TS_control
GPIO_Out	GPIO1_28_Out	GPIO1_29_Out	GPIO1_30_Out	GPIO1_31_Out
GPIO_In	GPIO1_28_In	GPIO1_29_In	GPIO1_30_In (PS2Clockin)	GPIO1_31_In (PS2Datain)
Pad Signals				
Module Pin Name	PA6	PA7	KBCLK	KBDATA

2.3. GPIO2

GPIO Signals	Bit0	Bit1	Bit2	Bit3
Alt_Output_1	PCIC_IORDB	PCIC_IOWRB	PCIC_OEB	PCIC_WEB
Alt_Output_2	Low	Low	Low	Low
Alt_Output_3	Low	Low	Low	Low
Alt_TS_Control_1	High	High	High	High
Alt_TS_Control_2	Low	Low	Low	Low
Alt_TS_Control_3	Low	Low	Low	Low
Alt_Receive_1	Low	Low	Low	Low
Alt_Receive_2	Low	Low	Low	Low
Alt_Receive_3	Low	Low	Low	Low
Alt_Input_1	Open	Open	Open	Open
Alt_Input_2	Open	Open	Open	Open
Alt_Input_3	Open	Open	Open	Open
GPIO_TS_control	GPIO2_0_TS_control	GPIO2_1_TS_control	GPIO2_2_TS_control	GPIO2_3_TS_control
GPIO_Out	GPIO2_0_Out	GPIO2_1_Out	GPIO2_2_Out	GPIO2_3_Out
GPIO_In	GPIO2_0_In	GPIO2_1_In	GPIO2_2_In	GPIO2_3_In
Pad Signals				
Module Pin Name	PCIORDN	PCIORRN	PCOEN	PCWEN

GPIO Signals	Bit4	Bit5	Bit6	Bit7
Alt_Output_1	PCIC_REGB	PCIC_POEB	PCIC_CE01B	PCIC_CE02B
Alt_Output_2	Low	Low	Low	Low
Alt_Output_3	Low	Low	Low	Low
Alt_TS_Control_1	High	High	High	High
Alt_TS_Control_2	Low	Low	Low	Low
Alt_TS_Control_3	Low	Low	Low	Low
Alt_Receive_1	Low	Low	Low	Low
Alt_Receive_2	Low	Low	Low	Low
Alt_Receive_3	Low	Low	Low	Low
Alt_Input_1	Open	Open	Open	Open
Alt_Input_2	Open	Open	Open	Open
Alt_Input_3	Open	Open	Open	Open
GPIO_TS_control	GPIO2_4_TS_control	GPIO2_5_TS_control	GPIO2_6_TS_control	GPIO2_7_TS_control
GPIO_Out	GPIO2_4_Out	GPIO2_5_Out	GPIO2_6_Out	GPIO2_7_Out
GPIO_In	GPIO2_4_In	GPIO2_5_In	GPIO2_6_In	GPIO2_7_In
Pad Signals				
Module Pin Name	PCREGN	PCPOEBN	PCCE01N	PCCE02N

GPIO Signals	Bit8	Bit9	Bit10	Bit11
Alt_Output_1	PCIC_RESET0	Low	Low	Low
Alt_Output_2	Low	Low	Low	Low
Alt_Output_3	Low	Low	Low	Low
Alt_TS_Control_1	High	Low	Low	Low
Alt_TS_Control_2	Low	Low	Low	Low
Alt_TS_Control_3	Low	Low	Low	Low
Alt_Receive_1	Low	Low	Low	Low
Alt_Receive_2	Low	Low	Low	Low
Alt_Receive_3	Low	Low	Low	Low
Alt_Input_1	Open	Open	Open	Open
Alt_Input_2	Open	Open	Open	Open
Alt_Input_3	Open	Open	Open	Open
GPIO_TS_control	GPIO2_8_TS_control	GPIO2_9_TS_control	GPIO2_10_TS_control	GPIO2_11_TS_control
GPIO_Out	GPIO2_8_Out	GPIO2_9_Out	GPIO2_10_Out	GPIO2_11_Out
GPIO_In	GPIO2_8_In	GPIO2_9_In (PCIC_CD01B)	GPIO2_10_In (PCIC_CD02B)	GPIO2_11_In (PCIC_VS01B)
Pad Signals				
Module Pin Name	PCRST0	PCCD01	PCCD02	PCVS01

GPIO Signals	Bit12	Bit13	Bit14	Bit15
Alt_Output_1	Low	Low	Low	Low
Alt_Output_2	Low	Low	Low	Low
Alt_Output_3	Low	Low	Low	Low

Alt_TS_Control_1	Low	Low	Low	Low
Alt_TS_Control_2	Low	Low	Low	Low
Alt_TS_Control_3	Low	Low	Low	Low
Alt_Receive_1	Low	Low	Low	Low
Alt_Receive_2	Low	Low	Low	Low
Alt_Receive_3	Low	Low	Low	Low
Alt_Input_1	Open	Open	Open	Open
Alt_Input_2	Open	Open	Open	Open
Alt_Input_3	Open	Open	Open	Open
GPIO_TS_control	GPIO2_12_TS_control	GPIO2_13_TS_control	GPIO2_14_TS_control	GPIO2_15_TS_control
GPIO_Out	GPIO2_12_Out	GPIO2_13_Out	GPIO2_14_Out	GPIO2_15_Out
GPIO_In	GPIO2_12_In (PCIC_VS02B)	GPIO2_13_In (PCIC_BVD01B)	GPIO2_14_In (PCIC_BVD02B)	GPIO2_15_In (PCIC_WP0)
Pad Signals				
Module Pin Name	PCVS02	PCBVD01	PCBVD02	PCWP0

GPIO Signals	Bit16	Bit17	Bit18	Bit19
Alt_Output_1	PCIC_CE11B	PCIC_CE12B	Low	Low
Alt_Output_2	Low	Low	Low	Low
Alt_Output_3	Low	Low	Low	Low
Alt_TS_Control_1	High	High	Low	Low
Alt_TS_Control_2	Low	Low	Low	Low
Alt_TS_Control_3	Low	Low	Low	Low
Alt_Receive_1	Low	Low	Low	Low
Alt_Receive_2	Low	Low	Low	Low
Alt_Receive_3	Low	Low	Low	Low
Alt_Input_1	Open	Open	Open	Open
Alt_Input_2	Open	Open	Open	Open
Alt_Input_3	Open	Open	Open	Open
GPIO_TS_control	GPIO2_16_TS_control	GPIO2_17_TS_control	GPIO2_18_TS_control	GPIO2_19_TS_control
GPIO_Out	GPIO2_16_Out	GPIO2_17_Out	GPIO2_18_Out	GPIO2_19_Out
GPIO_In	GPIO2_16_In	GPIO2_17_In	GPIO2_18_In (PCIC_RDYBSY0B)	GPIO2_19_In (PCIC_RDYBSY1B)
Pad Signals				
Module Pin Name	PCCE11N	PCCE12N	PCRDY0	PCRDY1

GPIO Signals	Bit20	Bit21	Bit22	Bit23
Alt_Output_1	Low	Low	Low	Low
Alt_Output_2	Low	Low	Low	Low
Alt_Output_3	Low	Low	Low	Low
Alt_TS_Control_1	Low	Low	Low	Low
Alt_TS_Control_2	Low	Low	Low	Low
Alt_TS_Control_3	Low	Low	Low	Low
Alt_Receive_1	Low	Low	Low	Low
Alt_Receive_2	Low	Low	Low	Low
Alt_Receive_3	Low	Low	Low	Low
Alt_Input_1	Open	Open	Open	Open
Alt_Input_2	Open	Open	Open	Open
Alt_Input_3	Open	Open	Open	Open
GPIO_TS_control	GPIO2_20_TS_control	GPIO2_21_TS_control	GPIO2_22_TS_control	GPIO2_23_TS_control
GPIO_Out	GPIO2_20_Out	GPIO2_21_Out	GPIO2_22_Out	GPIO2_23_Out
GPIO_In	GPIO2_20_In (In_interrupt0)	GPIO2_21_In (In_interrupt1)	GPIO2_22_In (In_interrupt2)	GPIO2_23_In (In_interrupt3)
Pad Signals				
Module Pin Name	IRQ0	IRQ1	IRQ2	IRQ3

GPIO Signals	Bit24	Bit25	Bit26	Bit27
Alt_Output_1	Low	Low	Low	PHOSTN
Alt_Output_2	Low	Low	Low	Low
Alt_Output_3	Low	Low	Low	Low
Alt_TS_Control_1	Low	Low	Low	High
Alt_TS_Control_2	Low	Low	Low	Low
Alt_TS_Control_3	Low	Low	Low	Low
Alt_Receive_1	Low	Low	Low	Low

Alt_Receive_2	Low	Low	Low	Low
Alt_Receive_3	Low	Low	Low	Low
Alt_Input_1	Open	PWAIT0N_sel	PWAIT1N_sel	Open
Alt_Input_2	Open	Open	Open	Open
Alt_Input_3	Open	Open	Open	Open
GPIO_TS_control	GPIO2_24_TS_control	GPIO2_25_TS_control	GPIO2_26_TS_control	GPIO2_27_TS_control
GPIO_Out	GPIO2_24_Out	GPIO2_25_Out	GPIO2_26_Out	GPIO2_27_Out
GPIO_In	GPIO2_24_In (In_interrupt4)	GPIO2_25_In (In_interrupt5, PWAIT0N)	GPIO2_26_In (In_interrupt6, PWAIT1N)	GPIO2_27_In (GPIO1_14_Alt_Receive_1)
Pad Signals				
Module Pin Name	IRQ4	IRQ5	IRQ6	PHOSTN

GPIO Signals	Bit28	Bit29	Bit30	Bit31
Alt_Output_1	Low	IRDA_Txd	Xcvroff	Low
Alt_Output_2	Low	UART2_TX	UART2_RTS	Low
Alt_Output_3	Low	Low	Low	Low
Alt_TS_Control_1	Low	High	High	Low
Alt_TS_Control_2	Low	High	High	Low
Alt_TS_Control_3	Low	Low	Low	Low
Alt_Receive_1	Ird_uart_rxd	Low	Low	Low
Alt_Receive_2	Low	Low	Low	Low
Alt_Receive_3	Low	Low	Low	Low
Alt_Input_1	UART2_RX	Open	Open	Open
Alt_Input_2	Open	Open	Open	Open
Alt_Input_3	Open	Open	Open	Open
GPIO_TS_control	GPIO2_28_TS_control	GPIO2_29_TS_control	GPIO2_30_TS_control	GPIO2_31_TS_control
GPIO_Out	GPIO2_28_Out	GPIO2_29_Out	GPIO2_30_Out	GPIO2_31_Out
GPIO_In	GPIO2_28_In (IRDA_Rxd)	GPIO2_29_In	GPIO2_30_In	GPIO2_31_In (UART2_CTS)
Pad Signals				
Module Pin Name	IRDARX	IRDATX	IRDACTR	CTS2N

2.4. GPIO3

GPIO Signals	Bit0	Bit1	Bit2	Bit3
Alt_Output_1	Low	UART1_TX	UART1_RTS_N	Low
Alt_Output_2	Low	HDLC1_TXD	HDLC1_TxRTSB	Low
Alt_Output_3	Low	Low	Low	Low
Alt_TS_Control_1	Low	High	High	Low
Alt_TS_Control_2	Low	High	High	Low
Alt_TS_Control_3	Low	Low	Low	Low
Alt_Receive_1	Low	Low	Low	Low
Alt_Receive_2	Low	Low	Low	Low
Alt_Receive_3	Low	Low	Low	Low
Alt_Input_1	Open	Open	Open	Open
Alt_Input_2	Open	Open	Open	Open
Alt_Input_3	Open	Open	Open	Open
GPIO_TS_control	GPIO3_0_TS_control	GPIO3_1_TS_control	GPIO3_2_TS_control	GPIO3_3_TS_control
GPIO_Out	GPIO3_0_Out	GPIO3_1_Out	GPIO3_2_Out	GPIO3_3_Out
GPIO_In	GPIO3_0_In (UART1_RX, HDLC1_RXD)	GPIO3_1_In	GPIO3_2_In	GPIO3_3_In (UART1_CTS, HDLC1_CTS)
Pad Signals				
Module Pin Name	RXD1	TXD1	RTS1N	CTS1N

GPIO Signals	Bit4	Bit5	Bit6	Bit7
Alt_Output_1	Low	Low	UART1_DTR_N	Low
Alt_Output_2	Low	Low	HDLC1_TxCLK_OUT	Low
Alt_Output_3	Low	Low	Low	Low
Alt_TS_Control_1	Low	Low	High	Low
Alt_TS_Control_2	Low	Low	HDLC1_TxCLK_OUT EN	Low
Alt_TS_Control_3	Low	Low	Low	Low
Alt_Receive_1	Low	Low	Low	Low
Alt_Receive_2	Low	Low	Low	Low
Alt_Receive_3	Low	Low	Low	Low
Alt_Input_1	Open	Open	Open	Open
Alt_Input_2	Open	Open	Open	Open
Alt_Input_3	Open	Open	Open	Open
GPIO_TS_control	GPIO3_4_TS_control	GPIO3_5_TS_control	GPIO3_6_TS_control	GPIO3_7_TS_control
GPIO_Out	GPIO3_4_Out	GPIO3_5_Out	GPIO3_6_Out	GPIO3_7_Out
GPIO_In	GPIO3_4_In (UART1_DCD, HDLC1_CD)	GPIO3_5_In (UART1_DSR, HDLC1_RCLK)	GPIO3_6_In (HDLC1_TxCLK_IN)	GPIO3_7_In (UART1_RI, HDLC0_CD)
Pad Signals				
Module Pin Name	DCD1N	DSR1N	DTR1N	RI1N

GPIO Signals	Bit8	Bit9	Bit10	Bit11
Alt_Output_1	DU	Low	Low	Low
Alt_Output_2	Low	HDLC0_TXD	Low	HDLC0_TxCLK_OUT
Alt_Output_3	Low	Low	Low	Low
Alt_TS_Control_1	High	Low	Low	Low
Alt_TS_Control_2	Low	High	Low	HDLC0_TxCLK_OUT EN
Alt_TS_Control_3	Low	Low	Low	Low
Alt_Receive_1	Low	Low	Low	Low
Alt_Receive_2	Low	Low	Low	Low
Alt_Receive_3	Low	Low	Low	Low
Alt_Input_1	Open	Open	Open	Open
Alt_Input_2	Open	Open	Open	Open
Alt_Input_3	Open	Open	Open	Open
GPIO_TS_control	GPIO3_8_TS_control	GPIO3_9_TS_control	GPIO3_10_TS_control	GPIO3_11_TS_control
GPIO_Out	GPIO3_8_Out	GPIO3_9_Out	GPIO3_10_Out	GPIO3_11_Out
GPIO_In	GPIO3_8_In (HDLC0_RXD)	GPIO3_9_In (DD)	GPIO3_10_In (DCL, HDLC0_RCLK)	GPIO3_11_In (FSC, HDLC0_TxCLK_IN)
Pad Signals				

Module Pin Name	IOM2DU	IOM2DD	IOM2DCL	IOM2FSC
GPIO Signals	Bit12	Bit13	Bit14	Bit15
Alt_Output_1	Low	Low	SCCLK	Low
Alt_Output_2	HDLC0_TxRTSB	Low	Low	Low
Alt_Output_3	Low	Low	Low	Low
Alt_TS_Control_1	Low	Low	High	Low
Alt_TS_Control_2	High	Low	Low	Low
Alt_TS_Control_3	Low	Low	Low	Low
Alt_Receive_1	Low	Low	Low	Low
Alt_Receive_2	Low	Low	Low	Low
Alt_Receive_3	Low	Low	Low	Low
Alt_Input_1	Open	Open	Open	Open
Alt_Input_2	Open	Open	Open	Open
Alt_Input_3	Open	Open	Open	Open
GPIO_TS_control	GPIO3_12_TS_control	GPIO3_13_TS_control	GPIO3_14_TS_control	GPIO3_15_TS_control
GPIO_Out	GPIO3_12_Out	GPIO3_13_Out	GPIO3_14_Out	GPIO3_15_Out
GPIO_In	GPIO3_12_In	GPIO3_13_In (HDLC0_CTS)	GPIO3_14_In	GPIO3_15_In (SCDET)
Pad Signals				
Module Pin Name	HRTS0N	HCTS0N	SCCLK	SCDET

GPIO Signals	Bit16	Bit17	Bit18	Bit19
Alt_Output_1	SCIO_out	SCRST	SCVEN	OUTPDWN
Alt_Output_2	Low	Low	Low	Low
Alt_Output_3	Low	Low	Low	Low
Alt_TS_Control_1	SC_DTSC	High	High	High
Alt_TS_Control_2	Low	Low	Low	Low
Alt_TS_Control_3	Low	Low	Low	Low
Alt_Receive_1	Low	Low	Low	Low
Alt_Receive_2	Low	Low	Low	Low
Alt_Receive_3	Low	Low	Low	Low
Alt_Input_1	Open	Open	Open	Open
Alt_Input_2	Open	Open	Open	Open
Alt_Input_3	Open	Open	Open	Open
GPIO_TS_control	GPIO3_16_TS_control	GPIO3_17_TS_control	GPIO3_18_TS_control	GPIO3_19_TS_control
GPIO_Out	GPIO3_16_Out	GPIO3_17_Out	GPIO3_18_Out	GPIO3_19_Out
GPIO_In	GPIO3_16_In (SCIO_in)	GPIO3_17_In	GPIO3_18_In	GPIO3_19_In
Pad Signals				
Module Pin Name	SCIO	SCRST	SCVEN	PNLOPD

GPIO Signals	Bit20	Bit21	Bit22	Bit23
Alt_Output_1	OUTX0	OUTX1	OUTY0	OUTY1
Alt_Output_2	Low	Low	Low	Low
Alt_Output_3	Low	Low	Low	Low
Alt_TS_Control_1	High	High	High	High
Alt_TS_Control_2	Low	Low	Low	Low
Alt_TS_Control_3	Low	Low	Low	Low
Alt_Receive_1	Low	Low	Low	Low
Alt_Receive_2	Low	Low	Low	Low
Alt_Receive_3	Low	Low	Low	Low
Alt_Input_1	Open	Open	Open	Open
Alt_Input_2	Open	Open	Open	Open
Alt_Input_3	Open	Open	Open	Open
GPIO_TS_control	GPIO3_20_TS_control	GPIO3_21_TS_control	GPIO3_22_TS_control	GPIO3_23_TS_control
GPIO_Out	GPIO3_20_Out	GPIO3_21_Out	GPIO3_22_Out	GPIO3_23_Out
GPIO_In	GPIO3_20_In	GPIO3_21_In	GPIO3_22_In	GPIO3_23_In
Pad Signals				
Module Pin Name	PNLOX0	PNLOX1	PNLOY0	PNLOY1

GPIO Signals	Bit24	Bit25	Bit26	Bit27
Alt_Output_1	Low	UART0_TX	UART0_RTS_N	Low
Alt_Output_2	Low	Low	Low	Low

Alt_Output_3	Low	Low	Low	Low
Alt_TS_Control_1	Low	High	High	Low
Alt_TS_Control_2	Low	Low	Low	Low
Alt_TS_Control_3	Low	Low	Low	Low
Alt_Receive_1	GPIO4_7_In	Low	Low	GPIO4_4_In
Alt_Receive_2	Low	Low	Low	Low
Alt_Receive_3	Low	Low	Low	Low
Alt_Input_1	UART0_RX	Open	Open	UART0_CTS
Alt_Input_2	Open	Open	Open	Open
Alt_Input_3	Open	Open	Open	Open
GPIO_TS_control	GPIO3_24_TS_control	GPIO3_25_TS_control	GPIO3_26_TS_control	GPIO3_27_TS_control
GPIO_Out	GPIO3_24_Out	GPIO3_25_Out	GPIO3_26_Out	GPIO3_27_Out
GPIO_In	GPIO3_24_In	GPIO3_25_In	GPIO3_26_In	GPIO3_27_In
Pad Signals				
Module Pin Name	RXD0	TXD0	RTS0N	CTS0N

GPIO Signals	Bit28	Bit29	Bit30	Bit31
Alt_Output_1	Low	Low	UART0_DTR_N	Low
Alt_Output_2	Low	SCP_DO	SCPCLKO	Low
Alt_Output_3	Low	Low	Low	Low
Alt_TS_Control_1	Low	Low	High	Low
Alt_TS_Control_2	Low	High	High	Low
Alt_TS_Control_3	Low	Low	Low	Low
Alt_Receive_1	Low	Low	Low	Low
Alt_Receive_2	Low	Low	Low	Low
Alt_Receive_3	Low	Low	Low	Low
Alt_Input_1	Open	Open	Open	Open
Alt_Input_2	Open	Open	Open	Open
Alt_Input_3	Open	Open	Open	Open
GPIO_TS_control	GPIO3_28_TS_control	GPIO3_29_TS_control	GPIO3_30_TS_control	GPIO3_31_TS_control
GPIO_Out	GPIO3_28_Out	GPIO3_29_Out	GPIO3_30_Out	GPIO3_31_Out
GPIO_In	GPIO3_28_In (UART0_DCD, SCP_DI)	GPIO3_29_In (UART0_DSR)	GPIO3_30_In	GPIO3_31_In (UART0_RI)
Pad Signals				
Module Pin Name	DCD0N	DSR0N	DTR0N	RI0N

2.5. GPIO4

GPIO Signals	Bit0	Bit1	Bit2	Bit3
Alt_Output_1	PDataOut0	PDataOut1	PDataOut2	PDataOut3
Alt_Output_2	Low	Low	Low	Low
Alt_Output_3	Low	Low	Low	Low
Alt_TS_Control_1	PDIR_N	PDIR_N	PDIR_N	PDIR_N
Alt_TS_Control_2	Low	Low	Low	Low
Alt_TS_Control_3	Low	Low	Low	Low
Alt_Receive_1	Low	Low	Low	Low
Alt_Receive_2	Low	Low	Low	Low
Alt_Receive_3	Low	Low	Low	Low
Alt_Input_1	Open	Open	Open	Open
Alt_Input_2	Open	Open	Open	Open
Alt_Input_3	Open	Open	Open	Open
GPIO_TS_control	GPIO4_0_TS_control	GPIO4_1_TS_control	GPIO4_2_TS_control	GPIO4_3_TS_control
GPIO_Out	GPIO4_0_Out	GPIO4_1_Out	GPIO4_2_Out	GPIO4_3_Out
GPIO_In	GPIO4_0_In (PdataIn0)	GPIO4_1_In (PdataIn)	GPIO4_2_In (PdataIn2)	GPIO4_3_In (PdataIn3)
Pad Signals				
Module Pin Name	PRTD0	PRTD1	PRTD2	PRTD3

GPIO Signals	Bit4	Bit5	Bit6	Bit7
Alt_Output_1	PDataOut4	PDataOut5	PDataOut6	PDataOut7
Alt_Output_2	Low	Low	Low	Low
Alt_Output_3	Low	Low	Low	Low
Alt_TS_Control_1	PDIR_N	PDIR_N	PDIR_N	PDIR_N
Alt_TS_Control_2	Low	Low	Low	Low
Alt_TS_Control_3	Low	Low	Low	Low
Alt_Receive_1	Low	Low	Low	Low
Alt_Receive_2	Low	Low	Low	Low
Alt_Receive_3	Low	Low	Low	Low
Alt_Input_1	Open	Open	Open	Open
Alt_Input_2	Open	Open	Open	Open
Alt_Input_3	Open	Open	Open	Open
GPIO_TS_control	GPIO4_4_TS_control	GPIO4_5_TS_control	GPIO4_6_TS_control	GPIO4_7_TS_control
GPIO_Out	GPIO4_4_Out	GPIO4_5_Out	GPIO4_6_Out	GPIO4_7_Out
GPIO_In	GPIO4_4_In (GPIO3_27_Alt_Receive_1, PdataIn4)	GPIO4_5_In (PdataIn5)	GPIO4_6_In (PdataIn6)	GPIO4_7_In (GPIO3_24_Alt_Receive_1, PdataIn7)
Pad Signals				
Module Pin Name	PRTD4	PRTD5	PRTD6	PRTD7

GPIO Signals	Bit8	Bit9	Bit10	Bit11
Alt_Output_1	PPU_nAck_P	PPU_Busy_P	PPU_Perror_P	PPU_nStrobe_H
Alt_Output_2	Low	Low	Low	Low
Alt_Output_3	Low	Low	Low	Low
Alt_TS_Control_1	PPU_PERIPHERAL	PPU_PERIPHERAL	PPU_PERIPHERAL	PPU_HOST
Alt_TS_Control_2	Low	Low	Low	Low
Alt_TS_Control_3	Low	Low	Low	Low
Alt_Receive_1	Low	Low	Low	Low
Alt_Receive_2	Low	Low	Low	Low
Alt_Receive_3	Low	Low	Low	Low
Alt_Input_1	Open	Open	Open	Open
Alt_Input_2	Open	Open	Open	Open
Alt_Input_3	Open	Open	Open	Open
GPIO_TS_control	GPIO4_8_TS_control	GPIO4_9_TS_control	GPIO4_10_TS_control	GPIO4_11_TS_control
GPIO_Out	GPIO4_8_Out	GPIO4_9_Out	GPIO4_10_Out	GPIO4_11_Out
GPIO_In	GPIO4_8_In (PPU_nAck_H)	GPIO4_9_In (PPU_Busy_H)	GPIO4_10_In (PPU_Perror_H)	GPIO4_11_In (PPU_nStrobe_P)
Pad Signals				
Module Pin Name	PRTACKN	PRTBUSY	PRTPE	PRTSTBN

GPIO Signals	Bit12	Bit13	Bit14	Bit15
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GPIO (General purpose I/O Controller) Connections

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Alt_Output_1	PPH_Select_P	PPU_nAutoFd_H	PPU_nError_P	PPU_nSelectIn_H
Alt_Output_2	Low	Low	Low	UART0_TX
Alt_Output_3	Low	Low	Low	Low
Alt_TS_Control_1	PPU_PERIPHERAL	PPU_HOST	PPU_PERIPHERAL	PPU_HOST
Alt_TS_Control_2	Low	Low	Low	High
Alt_TS_Control_3	Low	Low	Low	Low
Alt_Receive_1	Low	Low	Low	Low
Alt_Receive_2	Low	Low	Low	Low
Alt_Receive_3	Low	Low	Low	Low
Alt_Input_1	Open	Open	Open	Open
Alt_Input_2	Open	Open	Open	Open
Alt_Input_3	Open	Open	Open	Open
GPIO_TS_control	GPIO4_12_TS_control	GPIO4_13_TS_control	GPIO4_14_TS_control	GPIO4_15_TS_control
GPIO_Out	GPIO4_12_Out	GPIO4_13_Out	GPIO4_14_Out	GPIO4_15_Out
GPIO_In	GPIO4_12_In (PPH_Select_H)	GPIO4_13_In (PPU_nAutoFd_P)	GPIO4_14_In (PPU_nError_H)	GPIO4_15_In (PPU_nSelectIn_P)
Pad Signals				
Module Pin Name	PRTSLCT	PRTAFN	PRERRN	PRTSIN

GPIO Signals	Bit16	Bit17	Bit18	Bit19
Alt_Output_1	PPU_nInit_H	PDIR_N	C405_trcEvenExecution Status0	C405_trcOddExecution Status0
Alt_Output_2	UART0_RTS_N	Low	Low	Low
Alt_Output_3	Low	Low	Low	Low
Alt_TS_Control_1	PPU_HOST	High	High	High
Alt_TS_Control_2	High	Low	Low	Low
Alt_TS_Control_3	Low	Low	Low	Low
Alt_Receive_1	Low	Low	Low	Low
Alt_Receive_2	Low	Low	Low	Low
Alt_Receive_3	Low	Low	Low	Low
Alt_Input_1	Open	Open	Open	Open
Alt_Input_2	Open	Open	Open	Open
Alt_Input_3	Open	Open	Open	Open
GPIO_TS_control	GPIO4_16_TS_control	GPIO4_17_TS_control	GPIO4_18_TS_control	GPIO4_19_TS_control
GPIO_Out	GPIO4_16_Out	GPIO4_17_Out	GPIO4_18_Out	GPIO4_19_Out
GPIO_In	GPIO4_16_In (PPU_nInit_P)	GPIO4_17_In	GPIO4_18_In	GPIO4_19_In
Pad Signals				
Module Pin Name	PRTIN	PRTDOENN	TS1E	TS1O

GPIO Signals	Bit20	Bit21	Bit22	Bit23
Alt_Output_1	C405_trcEvenExecution Status1	C405_trcOddExecution Status1	C405_trcTraceStatus0	C405_trcTraceStatus1
Alt_Output_2	Low	Low	Low	Low
Alt_Output_3	Low	Low	Low	Low
Alt_TS_Control_1	High	High	High	High
Alt_TS_Control_2	Low	Low	Low	Low
Alt_TS_Control_3	Low	Low	Low	Low
Alt_Receive_1	Low	Low	Low	Low
Alt_Receive_2	Low	Low	Low	Low
Alt_Receive_3	Low	Low	Low	Low
Alt_Input_1	Open	Open	Open	Open
Alt_Input_2	Open	Open	Open	Open
Alt_Input_3	Open	Open	Open	Open
GPIO_TS_control	GPIO4_20_TS_control	GPIO4_21_TS_control	GPIO4_22_TS_control	GPIO4_23_TS_control
GPIO_Out	GPIO4_20_Out	GPIO4_21_Out	GPIO4_22_Out	GPIO4_23_Out
GPIO_In	GPIO4_20_In	GPIO4_21_In	GPIO4_22_In	GPIO4_23_In
Pad Signals				
Module Pin Name	TS2E	TS2O	TS3	TS4

GPIO Signals	Bit24	Bit25	Bit26	Bit27
Alt_Output_1	C405_trcTraceStatus2	C405_trcTraceStatus3	C405_trcCycle	Low
Alt_Output_2	Low	Low	Low	Low
Alt_Output_3	Low	Low	Low	Low

Alt_TS_Control_1	High	High	High	Low
Alt_TS_Control_2	Low	Low	Low	Low
Alt_TS_Control_3	Low	Low	Low	Low
Alt_Receive_1	Low	Low	Low	Low
Alt_Receive_2	Low	Low	Low	Low
Alt_Receive_3	Low	Low	Low	Low
Alt_Input_1	Open	Open	Open	Open
Alt_Input_2	Open	Open	Open	Open
Alt_Input_3	Open	Open	Open	Open
GPIO_TS_control	GPIO4_24_TS_control	GPIO4_25_TS_control	GPIO4_26_TS_control	Open
GPIO_Out	GPIO4_24_Out	GPIO4_25_Out	GPIO4_26_Out	Open
GPIO_In	GPIO4_24_In	GPIO4_25_In	GPIO4_26_In	Low
Pad Signals				
Module Pin Name	TS5	TS6	TCLK	

GPIO Signals	Bit28	Bit29	Bit30	Bit31
Alt_Output_1	Low	Low	Low	Low
Alt_Output_2	Low	Low	Low	Low
Alt_Output_3	Low	Low	Low	Low
Alt_TS_Control_1	Low	Low	Low	Low
Alt_TS_Control_2	Low	Low	Low	Low
Alt_TS_Control_3	Low	Low	Low	Low
Alt_Receive_1	Low	Low	Low	Low
Alt_Receive_2	Low	Low	Low	Low
Alt_Receive_3	Low	Low	Low	Low
Alt_Input_1	Open	Open	Open	Open
Alt_Input_2	Open	Open	Open	Open
Alt_Input_3	Open	Open	Open	Open
GPIO_TS_control	Open	Open	Open	Open
GPIO_Out	Open	Open	Open	Open
GPIO_In	Low	Low	Low	High
Pad Signals				
Module Pin Name				

Note1 : Input signals are directly connected with pads. So Alt_input_1(2,3) are not used, those are open.

Note2 : GPIO4 bit27-bit31 show the LSI version number. This shows 00001 version.

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