

LC77700B

(PowerPC 405IAP Embedded Processor)

User's Manual

USB Host

(Universal Serial Bus Host Controller)

**Date:8/27/2001
Revision:0.9**

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序文

本マニュアルについて

本マニュアルは、USB Host インタフェースの概要、動作、インタフェース、タイミングなどの仕様の詳細を提供します。

読者対象

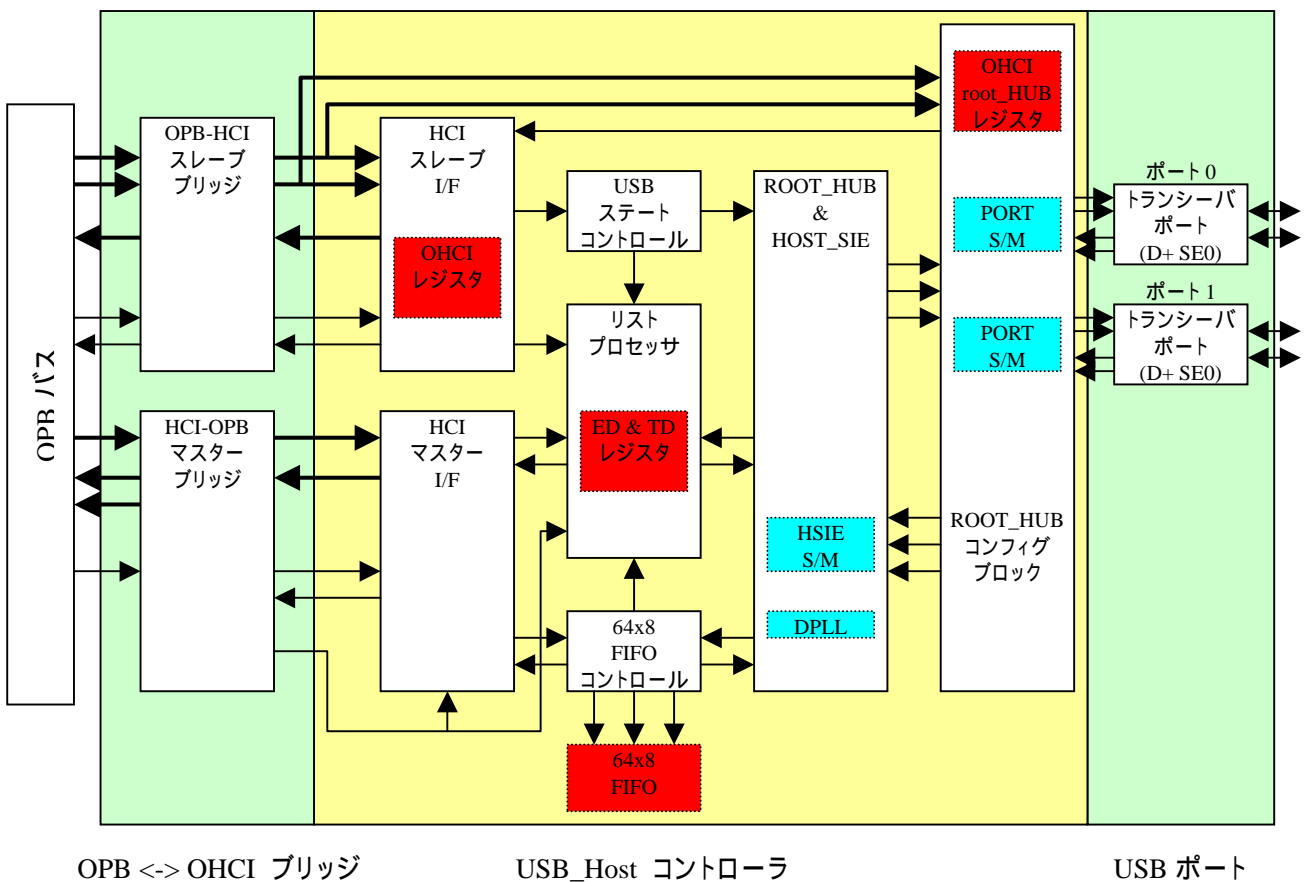
このマニュアルの対象読者は、USB Host インタフェースの理解する必要のあるハードウェア、ソフトウェア、アプリケーション開発担当者です。

1. 特徴

IBM OPBバスにインタフェースするUSB_HOSTインタフェースコントローラ IP で、以下の機能をサポートする。

- (1) USB Rev1.1 準拠。
- (2) Low_Speed & Full_Speed デバイスをサポート。
- (3) 2ポート
- (4) DPLL 内蔵。
- (5) OHCI:Open Host Controller Interface (業界標準バス) ⇔ OPB バスブリッジ により IBM_OPB に直結。(Master + Slave)
- (6) レベル割り込み
- (7) パワーマネジメント(mode1)対応

2. ブロック構成図



3. 信号の定義

3.1 USB HOST インタフェース

信号名	I/O	機能
PRT_RcvData	I	受信データ入力
PRT_RcvDPls	I	差動受信データ(+)
PRT_RcvDMns	O	差動受信データ(-)
RCFG_txDPls	O	送信データ出力
RCFG_txEnL	O	トランシーバ出力イネーブルコントロール出力
RCFG_speed	O	転送スピード切り替え信号 (トランシーバ特性の切り替え)
ROFG_se0	O	SE0(D+,D- = LL)
HCI_MIrqN	O	USB 割り込み (レベル)
Clk12	I	USB ホストコントローラ データ転送クロック
Clk48	I	USB ホストコントローラ メインクロック

3.2 OPB マスターインタフェース

信号名	I/O	機能
OPB_DBus	I	OPB データバス入力
OPB_MUHCGrant	I	OPB マスターグラント(許可)入力
OPB_xferAck	I	OPB 転送アクリッジ
OPB_fwAck	I	フルワード転送アクリッジ
OPB_hwAck	I	ハーフワード転送アクリッジ
OPB_timeout	I	OPB データ転送タイムアウト入力
OPB_retry	I	OPB データ転送 リトライ 入力
MUHC_ABus	O	USB_Master OPB バスロジック アドレスバス出力
MUHC_DBus	O	USB_Master OPB バスロジック データバス出力
MUHC_DBusEn	O	USB_Master OPB バスロジック データバスイネーブル出力
MUHC_request	O	USB_Master OPB バスロジック リクエスト出力
MUHC_buslock	O	USB_Master OPB バスロジック バスロック出力
MUHC_select	O	USB_Master OPB バスロジック セレクト出力
MUHC_RNW	O	USB_Master OPB バスロジック リード/ライト出力
MUHC_fwXfer	O	USB_Master OPB バスロジック フルワードアクセス出力
MUHC_hwXfer	O	USB_Master OPB バスロジック ハーフワードアクセス出力

3.3 OPB スレーブインタフェース

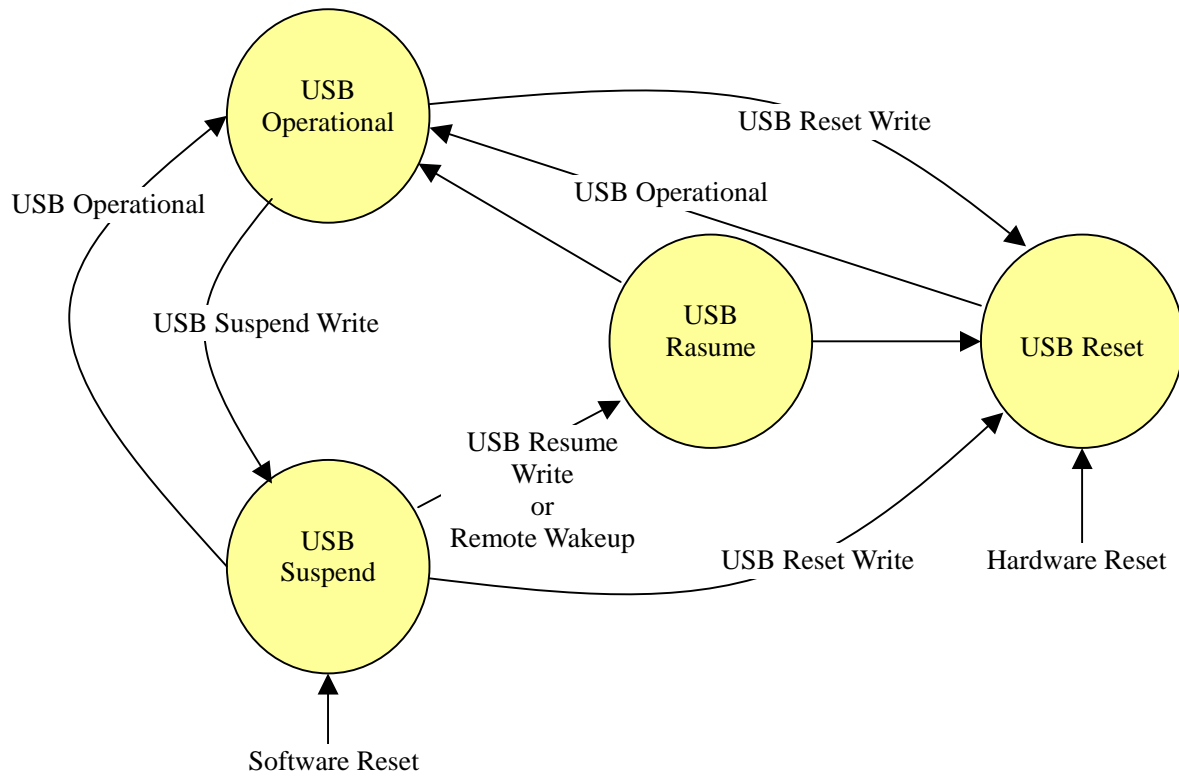
信号名	I/O	機能
OPB_DBus[0:31]	I	OPB データバス入力
OPB_ABus[0:31]	I	OPB アドレスバス入力
OPB_select	I	OPB セレクト信号入力 : 転送データが確定した事を示す信号
OPB_RNW	I	リード/ライト信号入力
OPB_fwXfer	I	OPB バスロジック full word 転送
SUHC_DBus[0:31]	O	USB_Slave OPB バスロジック データバス出力
SUHC_DBusEn	O	USB_Slave OPB バスロジック データバスイネーブル信号
SUHC_XferAck	O	USB_Slave OPB バスロジック アクリッジ信号
SUHC_fwAck	O	full word アクリッジ信号
SUHC_ToutSup	O	タイムアウトサブレス

3.4 システム信号

信号名	I/O	機能
sys_clk	I	システムクロック入力 (50MHz) OPB バスクロック
RSTB	I	リセット信号入力
CPM_Sleep_N	I	スリープ要求信号入力

4. 状態遷移図

動作状態は、大きく、下記の4状態で構成される。



USB Reset :

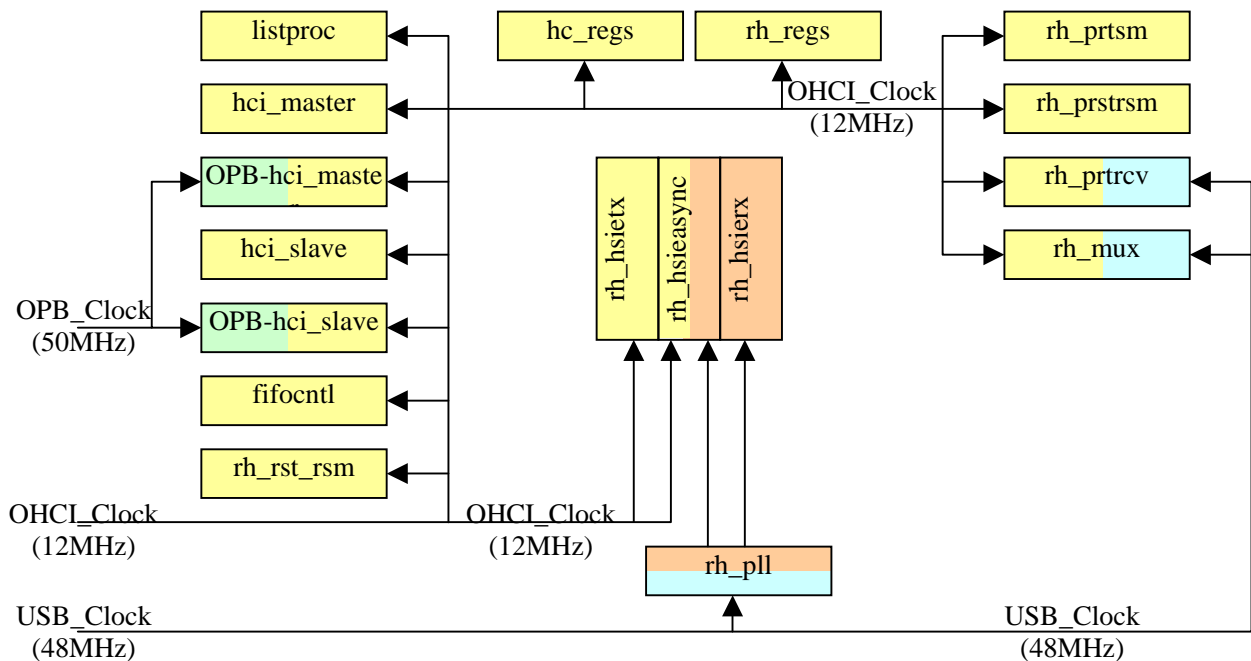
USB Suspend :

USB Rasume :

USB Operational :

5. クロック系統図

各ブロックで使用されるクロックは、下記の通りに構成される。



OPB_Clock(OPB バスクロック),OHCI_Clock(12MHz 固定),USB_Clock(48MHz 固定)の主要3クロックで動作する。

- (1) OPB_Clock :OPB バスクロックで最大 50MHz で動作する。
- (2) OHCI_Clock:USB 転送用のメインクロックで 12MHz 固定である。OHCI の基準クロックでもあります。
- (3) USB_Clock :USB_Host コントローラ全体のメインクロックで 48MHz 固定である。

6 . OHCI インタフェース

() OpenHCI インタフェース仕様の詳細は、
「Open Host Interface Specification for USB V1.1a」(COMPAQ)を、参照してください。

6.1 OHCI レジスタ (マスターインタフェース)

マスターインタフェースでは、USB_Host インタフェースでの USB 転送を規定する2つのパラメータ ED(Endpoint-Descriptor)/TD(Transfer-Descriptor)と、USB 転送データの送受が行われる。

USB バスに繋がる Endpoint に対応して、ED/TD を下図のように構成(リスト構造)しデータ転送を行う。

(USB_Host に内蔵されたリストプロセッサが、このリスト構造に基づいて、データ転送の制御を行う。)

6.1.1 ED/TD リスト構造

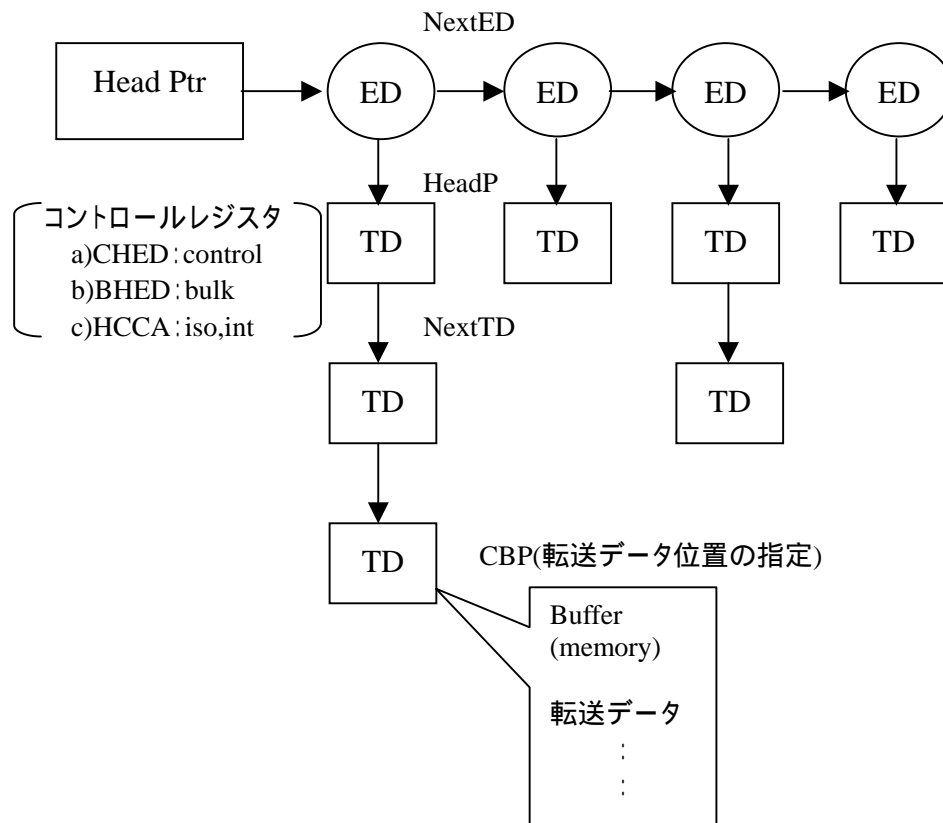


図 ED/TD リスト構造

6.1.2 ED/TD リスト構造(例)

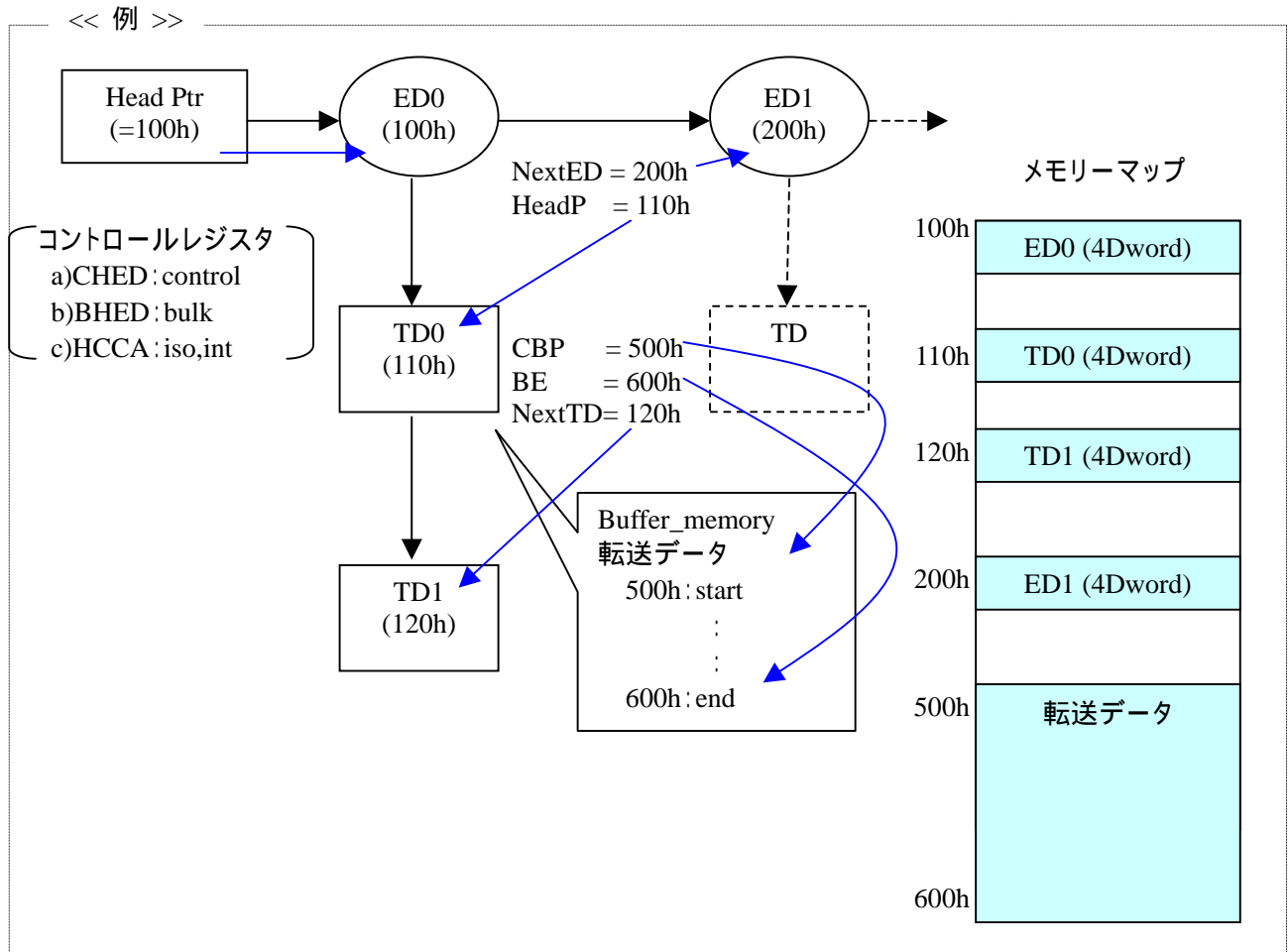


図 ED/TD リスト構造(例)

6.2 ED(Endpoint-Descriptor)の構成

転送の各 Endpoint 毎に定義される、16byte 単位のパラメータである。

	MSB										LSB					
	3	2	2	1	1	1	1	1	1	0	0	0	0	0	0	0
	1	7	6	6	5	4	3	2	1	0	7	6	4	3	2	1
Dword0	-		MPS			F	K	S	D	EN		FA				
Dword1	TD Queue Tail Pointer (TailP)												-			
Dword2	TD Queue Header Pointer (HeadP)												0*	C	H	
Dword3	Next Endpoint Descriptor (NextED)												-			

(注*) Fields containing ' 0 ' must be written to 0 by the Host Controller Driver before queued for Host Controller processing. If Host Controller has write access to the field, it will always write the field to 0.

レジスタ名	アクセス	説明										
FA	R	FunctionAddress This is the USB address of the function containing the endpoint that this ED controls										
EN	R	EndpointNumber This is the USB address of the endpoint within the function										
D	R	Direction This 2-bit field indicates the direction of data flow (IN or OUT.) If neither IN nor OUT is specified, then the direction is determined from the PID field of the TD. The encoding of the bits of this field are: <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>Code</th> <th>Direction</th> </tr> </thead> <tbody> <tr> <td>00</td> <td>Get direction from TD</td> </tr> <tr> <td>01</td> <td>Out</td> </tr> <tr> <td>10</td> <td>In</td> </tr> <tr> <td>11</td> <td>Get direction from TD</td> </tr> </tbody> </table>	Code	Direction	00	Get direction from TD	01	Out	10	In	11	Get direction from TD
Code	Direction											
00	Get direction from TD											
01	Out											
10	In											
11	Get direction from TD											
S	R	Speed Indicates the speed of the endpoint: full-speed (S = 0) or low-speed (S = 1.)										
K	R	sKip When this bit is set, the HC continues on to the next ED on the list without attempting access to the TD queue or issuing any USB token for the endpoint										
F	R	Format This bit indicates the format of the TDs linked to this ED. If this is a Control, Bulk, or Interrupt Endpoint, then F = 0, indicating that the General TD format is used. If this is an Isochronous Endpoint, then F = 1, indicating that the Isochronous TD format is used										
MPS	R	MaximumPacketSize This field indicates the maximum number of bytes that can be sent to or received from the endpoint in a single data packet										
TailP	R	TDQueueTailPointer If TailP and HeadP are the same, then the list contains no TD that the HC can process. If TailP and HeadP are different, then the list contains a TD to be processed										
H	R/W	Halted This bit is set by the HC to indicate that processing of the TD queue on the endpoint is halted, usually due to an error in processing a TD.										
C	R/W	toggleCarry This bit is the data toggle carry bit. Whenever a TD is retired, this bit is written to contain the last data toggle value (LSb of data Toggle field) from the retired TD. This field is not used for Isochronous Endpoints										
HeadP	R/W	TDQueueHeadPointer Points to the next TD to be processed for this endpoint.										
NextED	R	NextED If nonzero, then this entry points to the next ED on the list										

6.3 TD (Transfer-Descriptor)の構成

転送を行うEndpointのEDにリンクして定義される16byte単位の転送パラメータである。

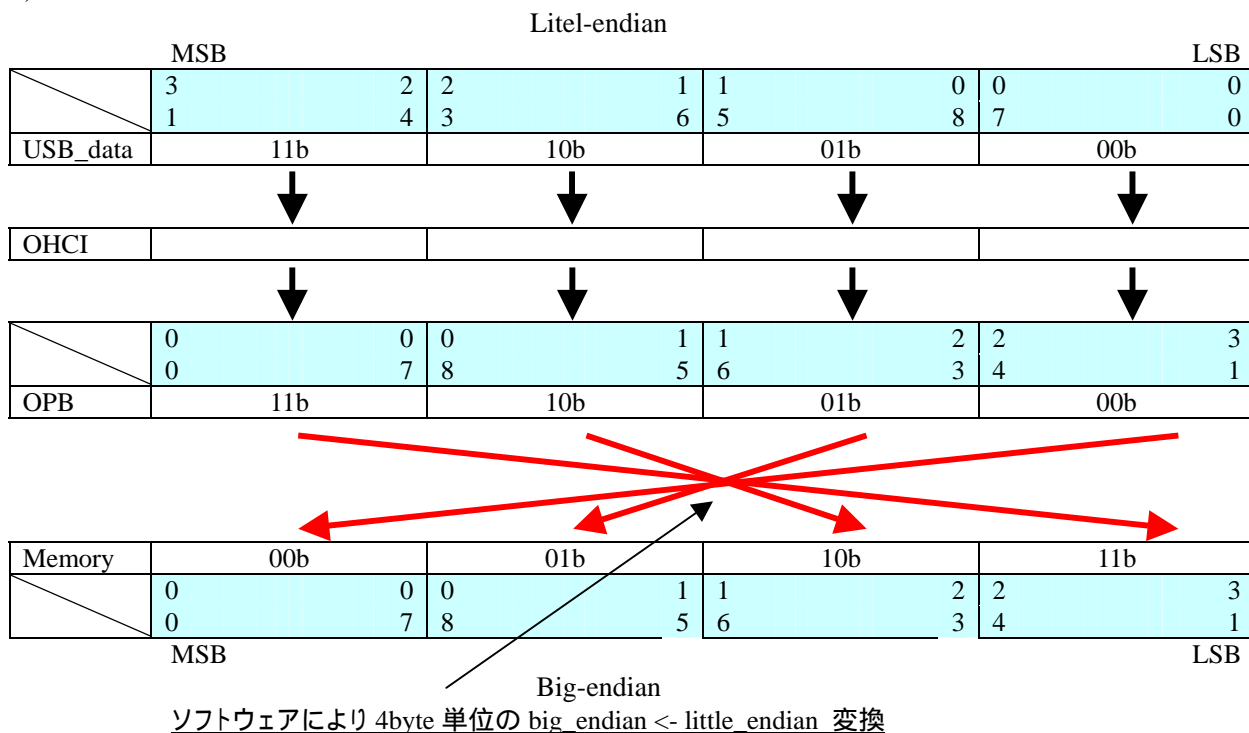
	MSB										LSB	
	3	2	2	2	2	2	2	1	1	1	0	0
	1	8	7	6	5	4	3	1	0	9	8	7
Dword0	CC		EC		T		DI		DP		R	
Dword1	Current Buffer Pointer (CBP)											
Dword2	Next TD (NextTD)											0
Dword3	Buffer End (BE)											

レジスタ名	アクセス	説明															
R	R	bufferRounding If this bit is 0, then the last data packet to a TD from an endpoint must exactly fill the defined data buffer. If the bit is 1, then the last data packet may be smaller than the defined buffer without causing an error condition on the TD.															
DP	R	Direction/PID This 2-bit field indicates the direction of data flow and the PID to be used for the token. This field is only relevant to the HC if the D field in the ED was set to 00b or 11b indicating that the PID determination is deferred to the TD. The encoding of the bits within the byte for this field are: <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>Code</th> <th>PID Type</th> <th>Data Direction</th> </tr> </thead> <tbody> <tr> <td>00</td> <td>Setup</td> <td>To endpoint</td> </tr> <tr> <td>01</td> <td>Out</td> <td>To endpoint</td> </tr> <tr> <td>10</td> <td>In</td> <td>From endpoint</td> </tr> <tr> <td>11</td> <td>Reserved</td> <td>-</td> </tr> </tbody> </table>	Code	PID Type	Data Direction	00	Setup	To endpoint	01	Out	To endpoint	10	In	From endpoint	11	Reserved	-
Code	PID Type	Data Direction															
00	Setup	To endpoint															
01	Out	To endpoint															
10	In	From endpoint															
11	Reserved	-															
DI	R	DelayInterrupt This field contains the interrupt delay count for this TD. When a TD is complete the HC may wait for DelayInterrupt frames before generating an interrupt. If DelayInterrupt is 111b, then there is no interrupt associated with completion of this TD.															
T	R/W	DataToggle This 2-bit field is used to generate/compare the data PID value (DATA0 or DATA1). It is updated after each successful transmission/reception of a data packet. The MSb of this field is '0' when the data toggle value is acquired from the toggleCarry field in the ED and '1' when the data toggle value is taken from the LSb of this field.															
EC	R/W	ErrorCount For each transmission error, this value is incremented. If ErrorCount is 2 and another error occurs, the error type is recorded in the ConditionCode field and placed on the done queue. When a transaction completes without error, ErrorCount is reset to 0.															
CC	R/W	ConditionCode This field contains the status of the last attempted transaction.															
CBP	R/W	CurrentBufferPointer Contains the physical address of the next memory location that will be accessed for transfer to/from the endpoint. A value of 0 indicates a zero-length data packet or that all bytes have been transferred.															
NextTD	R/W	NextTD This entry points to the next TD on the list of TDs linked to this endpoint															
BE	R	BufferEnd Contains physical address of the last byte in the buffer for this TD															

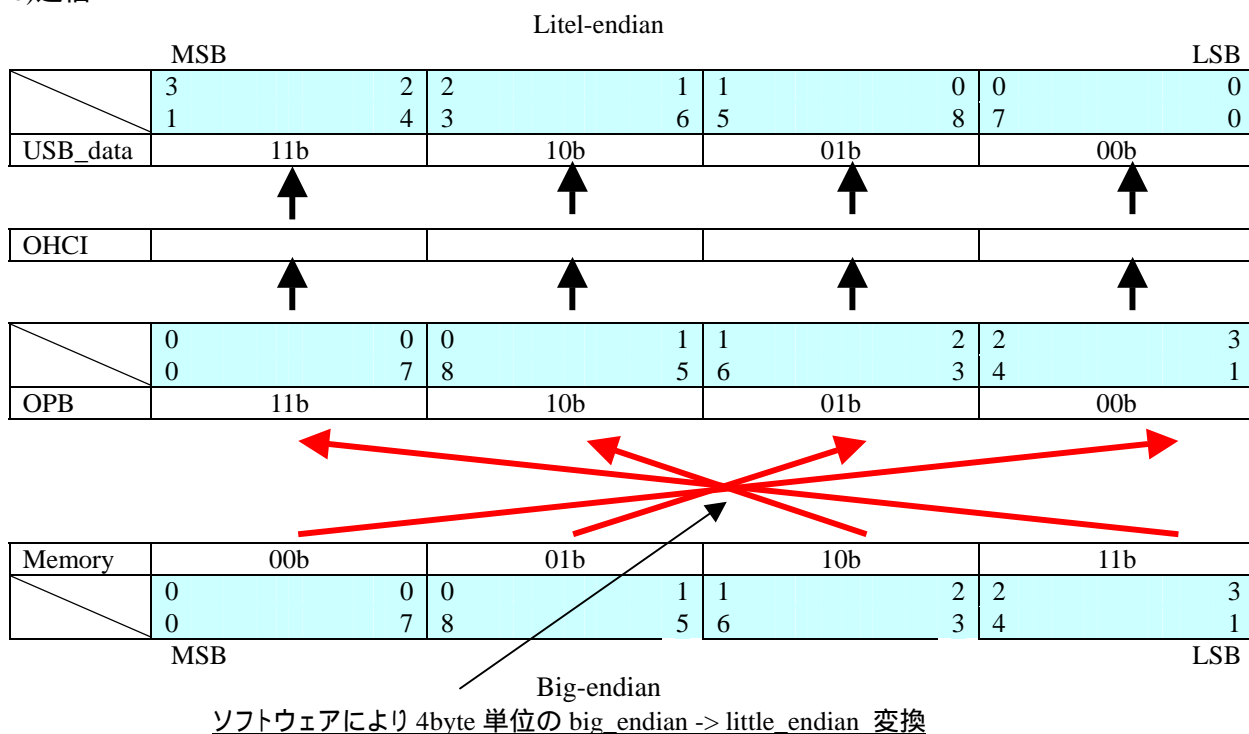
6.4 USB 転送データ

USB 転送データのデータフォーマットは、little_endian であり、OpenHCI インタフェース上も little_endian である。しかし、OPB バスは、big_endian(default)であるので、ソフトウェアにより 4byte 単位の big_endian <-> little_endian 変換が必要になる。

a)受信



b)送信



6.2 OHCI コントロールレジスタマップ (スレーブインタフェース)

USB ホスト コントローラ Operational レジスタ

アドレス		C
		C
0xEF601200	HcRevision	
0xEF601204	HcControl	
0xEF601208	HcCommandStatus	
0xEF60120C	HcInterruptStatus	
0xEF601210	HcInterruptEnable	
0xEF601214	HcInterruptDisable	
0xEF601218	HcHCCA	
0xEF60121C	HcPeriodCurrentED	
0xEF601220	HcControlHeadED	
0xEF601224	HcControlCurrentED	
0xEF601228	HcBulkHeadED	
0xEF60122C	HcBulkCurrentED	
0xEF601230	HcDoneHead	
0xEF601234	HcFmInterval	
0xEF601238	HcFmRemaining	
0xEF60123C	HcFmNumber	
0xEF601240	HcPeriodicStart	
0xEF601244	HcLSThreshold	
0xEF601248	HcRhDescriptorA	
0xEF60124C	HcRhDescriptorB	
0xEF601250	HcRhStatus	
0xEF601254	HcRhPortStatus[0]	
0xEF601258	HcRhPortStatus[1]	

) アドレス:0xEF601200 からに、マッピング。

6.3 レジスタ仕様

< 制御・状態 >

1) レビジョン レジスタ (+00)

3	0	0	0
1	8	7	0
reserved			REV

Key	Reset	Read/Write		Description
		HCD	HC	
REV	10h	R	R	Revision

2) 制御 レジスタ (+04)

3	1	1	0	0	0	0	0	0	0	0	0	0	0
1	1	0	9	8	7	6	5	4	3	2	1	0	0
reserved		R	R	I	H	B	C	I	P	C			
		W	W	R	C	L	L	E	L	B			
		E	C		F	E	E	E	S	R			

Key	Reset	Read/Write		Description										
		HCD	HC											
CBSR	00b	R/W	R	ControlBulkServiceRatio <table border="1"> <thead> <tr> <th>CBSR</th> <th>No. of Control EDs Over Bulk EDs Served</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>1 : 1</td> </tr> <tr> <td>1</td> <td>2 : 1</td> </tr> <tr> <td>2</td> <td>3 : 1</td> </tr> <tr> <td>3</td> <td>4 : 1</td> </tr> </tbody> </table>	CBSR	No. of Control EDs Over Bulk EDs Served	0	1 : 1	1	2 : 1	2	3 : 1	3	4 : 1
CBSR	No. of Control EDs Over Bulk EDs Served													
0	1 : 1													
1	2 : 1													
2	3 : 1													
3	4 : 1													
PLE	0b	R/W	R	PeriodicListEnable										
IE	0b	R/W	R	IsochronousEnable										
CLE	0b	R/W	R	ControlListEnable										
BLE	0b	R/W	R	BulkListEnable										
HCFS	00b	R/W	R/W	HostControllerFunctionalState for USB 00b: USBRESET 01b: USBRESUME 10b: USBOPERATIONAL 11b: USBSUSPEND										
IR	0b	R/W	R	InterruptRouting										
RWC	0b	R/W	R/W	RemoteWakeupConnected										
RWE	0b	R/W	R	RemoteWakeupEnable										

3) コマンドステータスレジスタ (+08)

3	1	1	1	0	0	0	0	0	
1	8	7	6	5	4	3	2	1	0
reserved				S O C	reserved				O B C H C L L C R F F R

Key	Reset	Read/Write		Description
		HCD	HC	
HCR	0b	R/W	R/W	HostControllerReset
CLF	0b	R/W	R/W	ControlListFilled
BLF	0b	R/W	R/W	BulkListFilled
OCR	0b	R/W	R/W	OwnershipChangeRequest
SOC	00b	R	R/W	SchedulingOverrunCount

4) 割り込みステータスレジスタ (+0c)

3	3	2	0	0	0	0	0	0	0	0			
1	0	9	7	6	5	4	3	2	1	0			
0	O C	reserved						R H S C	F H S O	U N E D	R E D F	S W D O	W S H

Key	Reset	Read/Write		Description
		HCD	HC	
SO	0b	R/W	R/W	SchedulingOverrun
WDH	0b	R/W	R/W	WritebackDoneHead
SF	0b	R/W	R/W	StartofFrame
RD	0b	R/W	R/W	ResumeDetected
UE	0b	R/W	R/W	UnrecoverableError
FNO	0b	R/W	R/W	FrameNumberOverflow
RHSC	0b	R/W	R/W	RootHubStatusChange
OC	0b	R/W	R/W	OwnershipChange

a) Memory Pointer Partition

7) HcHCCA Register (+18)

3	0	0	0
1	8	7	0
HCCA			0

Key	Reset	Read/Write		Description
		HCD	HC	
HCCA	0h	R/W	R	ホストコントローラの通信領域のベースアドレス

8) HcPeriodCurrentED Register (+1c)

3	0	0	0
1	4	3	0
PCED			0

Key	Reset	Read/Write		Description
		HCD	HC	
PCED	0h	R	R/W	PeriodCurrentED

9) HcControlHeadED Register (+20)

3	0	0	0
1	4	3	0
CHED			0

Key	Reset	Read/Write		Description
		HCD	HC	
CHED	0h	R/W	R	ControlHeadED

10) HcControlCurrentED Register (+24)

3	0	0	0
1	4	3	0
CCED			0

Key	Reset	Read/Write		Description
		HCD	HC	
CCED	0h	R/W	R/W	ControlCurrentED

11) HcBulkHeadED Register (+28)

3	0	0	0
1	4	3	0
BHED			0

Key	Reset	Read/Write		Description
		HCD	HC	
BHED	0h	R/W	R	BulkHeadED

12) HcBulkCurrentED Register (+2c)

3	0	0	0
1	4	3	0
BCED			0

Key	Reset	Read/Write		Description
		HCD	HC	
BCED	0h	R/W	R/W	BulkCurrentED

13) HcDoneHead Register (+30)

3	0	0	0
1	4	3	0
DH			0

Key	Reset	Read/Write		Description
		HCD	HC	
DH	0h	R	R/W	DoneHead

Frame Counter Partition

14) HcFmInterval Register (+34)

3	3	1	1	1	1	0
1	0	6	5	4	3	0
F	FSMPS				reserved	FI
I						
T						

Key	Reset	Read/Write		Description
		HCD	HC	
FI	2EDFh	R/W	R	FrameInterval
FSMPS	TBD	R/W	R	FSLargestDataPacket
FIT	0b	R/W	R	FrameIntervalToggle

15) HcFmRemaining Register (+38)

3	3	1	1	0	
1	0	4	3	0	
F	reserved				FR
R					
T					
0					0000h
R					R

Key	Reset	Read/Write		Description
		HCD	HC	
FR	0h	R	R/W	FrameRemaining
FRT	0b	R	R/W	FrameRemainingToggle

16) HcFmNumber Register (+3c)

3	1	1	0
1	6	5	0
reserved			FN

Key	Reset	Read/Write		Description
		HCD	HC	
FN	0h	R	R/W	FrameNumber

17) HcPeriodicStart Register (+40)

3	1	1	0
1	4	3	0
reserved		PS	

Key	Reset	Read/Write		Description
		HCD	HC	
PS	0h	R/W	R	PeriodicStart

18) HcLSThreshold Register (+44)

3	1	1	0
1	2	1	0
reserved		LST	

Key	Reset	Read/Write		Description
		HCD	HC	
LST	0628h	R/W	R	LSThreshold

Root Hub Partition

19) HcRhDescriptorA Register (+48)

3	2	2	1	1	1	1	0	0	0	0
1	4	3	3	2	1	0	9	8	7	0
POTPGT		Reserved			N	O	D	N	P	NDP
					O	C	T	P	S	
					C	P	S	M		
					P	M				

Field	Power On Reset	Read/Write		Description
		HCD	HC	
NDP	IS	R	R	NumberDownstreamPorts
NPS	IS	R/W	R	NoPowerSwitching 0: Ports are power switched 1: Ports are always powered on when the HC is powered on
PSM	IS	R/W	R	PowerSwitchingMode 0: all ports are powered at the same time. 1: each port is powered individually.
DT	0b	R	R	DeviceType
OCPM	IS	R/W	R	OverCurrentProtectionMode 0: over-current status is reported collectively for all downstream ports 1: over-current status is reported on a per-port basis
NOCP	IS	R/W	R	NoOverCurrentProtection 0: Over-current status is reported collectively for all downstream ports 1: No overcurrent protection supported
POTPGT	IS	R/W	R	PowerOnToPowerGoodTime The duration is calculated as POTPGT * 2 ms.

20) HcRhDescriptorB Register (+4c)

3	1	1	0
1	6	5	0
PPCM		DR	

Field	Power-On Reset	Read/Write		Description
		HCD	HC	
DR	IS	R/W	R	DeviceRemovable bit 0: Reserved bit 1: Device attached to Port #1 bit 2: Device attached to Port #2 ... bit15: Device attached to Port #15
PPCM	IS	R/W	R	PortPowerControlMask (PowerSwitchingMode=0), this field is not valid. bit 0: Reserved bit 1: Ganged-power mask on Port #1 bit 2: Ganged-power mask on Port #2 ... bit15: Ganged-power mask on Port #15

21) HcRhStatus Register (+50)

3	3	1	1	1	1	1	0	0	0
1	0	8	7	6	5	4	2	1	0
CRWE	Reserved			OLDC CPRI RISW CCCE	Reserved			OLDC CPRI RISW	

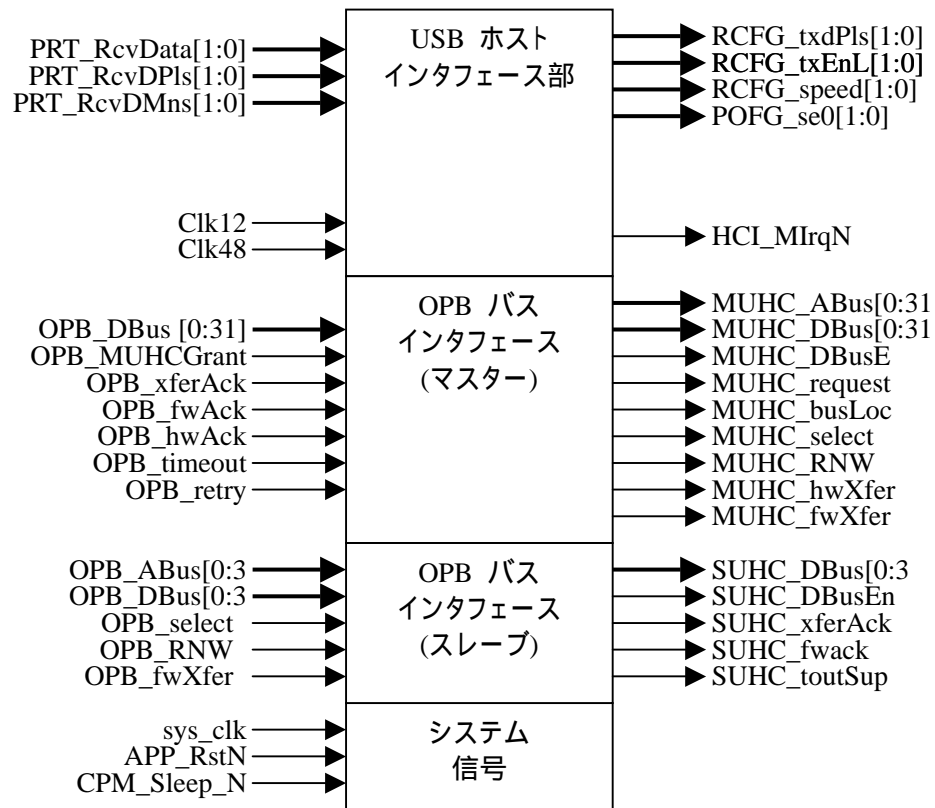
Field	Root Hub Reset	Read/Write		Description
		HCD	HC	
LPS	0b	R/W	R	(read) LocalPowerStatus (write) ClearGlobalPower
OCI	0b	R	R/W	OverCurrentIndicator
DRWE	0b	R/W	R	(read) DeviceRemoteWakeupEnable 0 = ConnectStatusChange is not a remote wakeup event. 1 = ConnectStatusChange is a remote wakeup event. (write) SetRemoteWakeupEnable '1' sets DeviceRemoveWakeupEnable . '0' has no effect.
LPSC	0b	R/W	R	(read) LocalPowerStatusChange (write) SetGlobalPower In global power mode (PowerSwitchingMode=0), This bit is written to '1' to turn on power to all ports (clear
CCIC	0b	R/W	R/W	OverCurrentIndicatorChange 1: clear 0: no effect.
CRWE	-	W	R	(write) ClearRemoteWakeupEnable 1: clears DeviceRemoveWakeupEnable . 0: no effect.

Field	Root Hub Reset	Read/Write		Description
		HCD	HC	
CSC	0b	R/W	R/W	ConnectStatusChange 0 = no change in CurrentConnectStatus 1 = change in CurrentConnectStatus Note: If the DeviceRemovable[NDP] bit is set, this bit is set only after a Root Hub reset to inform the system that the device is attached.
PESC	0b	R/W	R/W	PortEnableStatusChange 1: clear 0: no effect. 0 = no change in PortEnableStatus 1 = change in PortEnableStatus
PSSC	0b	R/W	R/W	PortSuspendStatusChange 1: clear 0: no effect 0 = resume is not completed 1 = resume completed
OCIC	0b	R/W	R/W	PortOverCurrentIndicatorChange 1: clear 0: no effect 0 = no change in PortOverCurrentIndicator 1 = PortOverCurrentIndicator has changed
PRSC	0b	R/W	R/W	PortResetStatusChange 0 = port reset is not complete 1 = port reset is complete

Open-HCI 規格 より 抜粋。

付録

<< USB HOST インタフェース 信号 >>



変更履歴:

2001.06.18: OPB バスマスターインタフェース(OHCI マスター)についての追加。
(USB 転送データは、big_endian <-> little_endian 変換が必要であることを明記。)

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